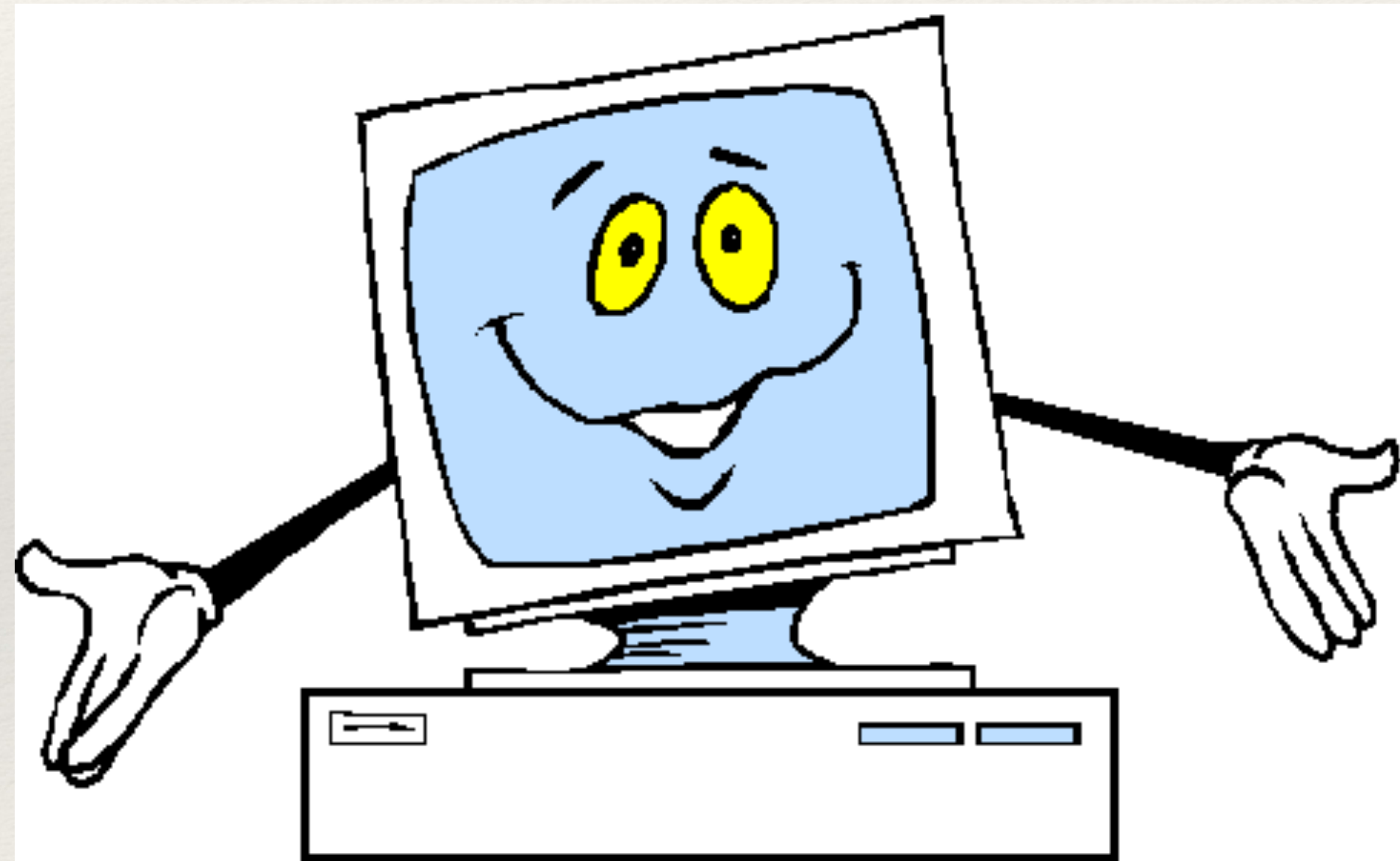


# Computers

## Logic and CPU

*Patrice Koehl  
Computer Science  
UC Davis*



# Computers

Logic: acting on information

The Central Processing Unit (CPU)

Elements of a Computer

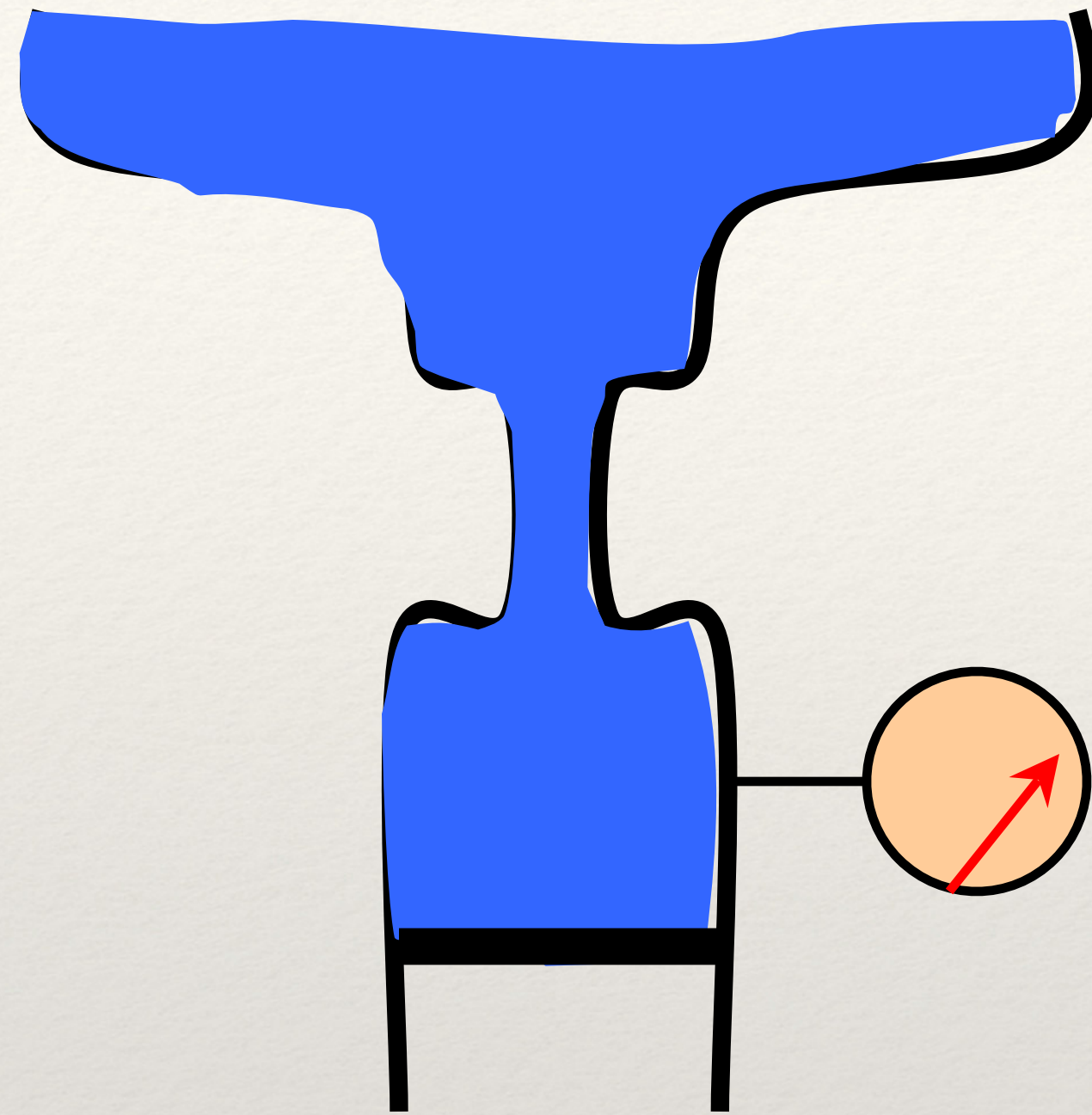
# Computers

Logic: acting on information

The Central Processing Unit (CPU)

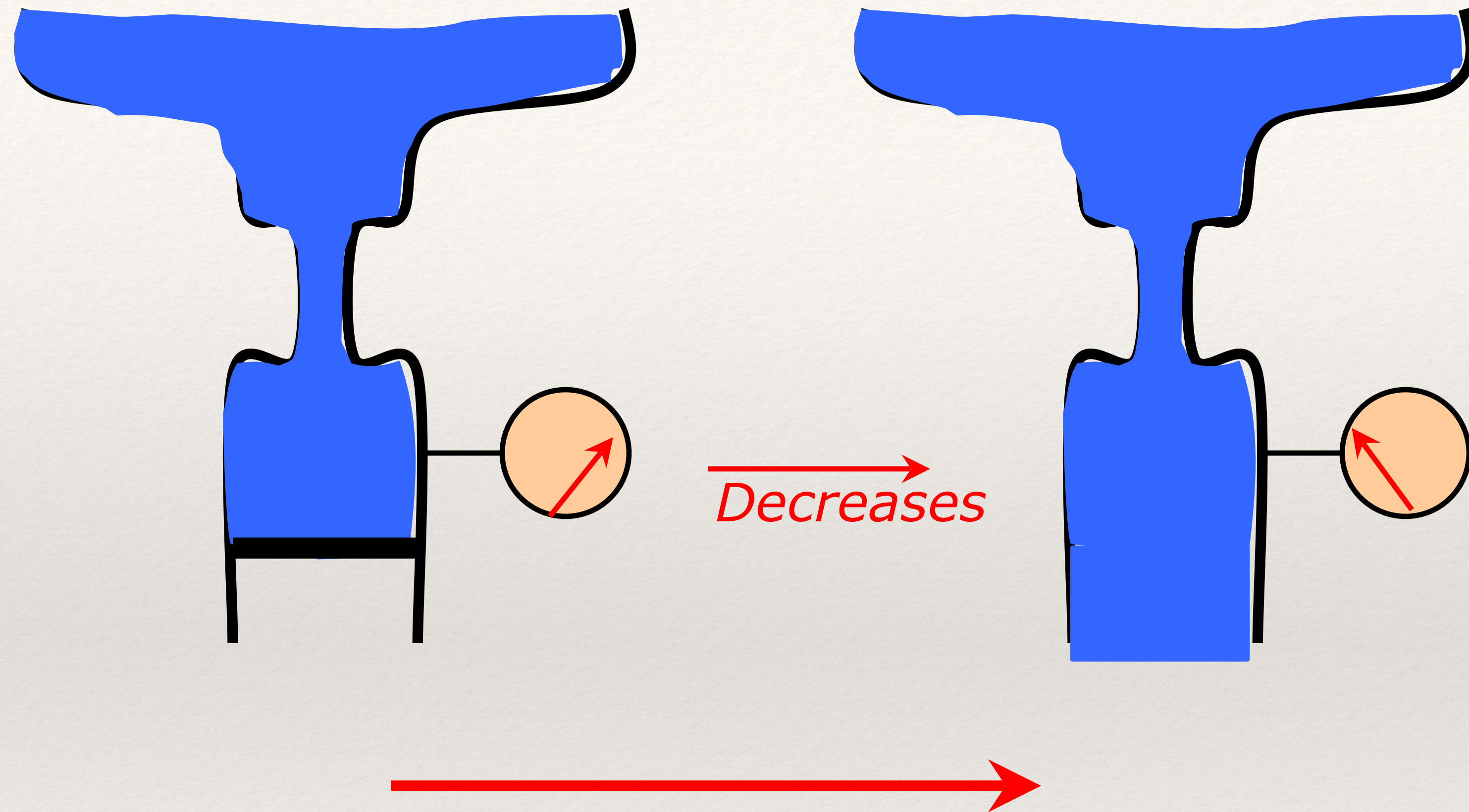
Elements of a Computer

# The concept of pressure



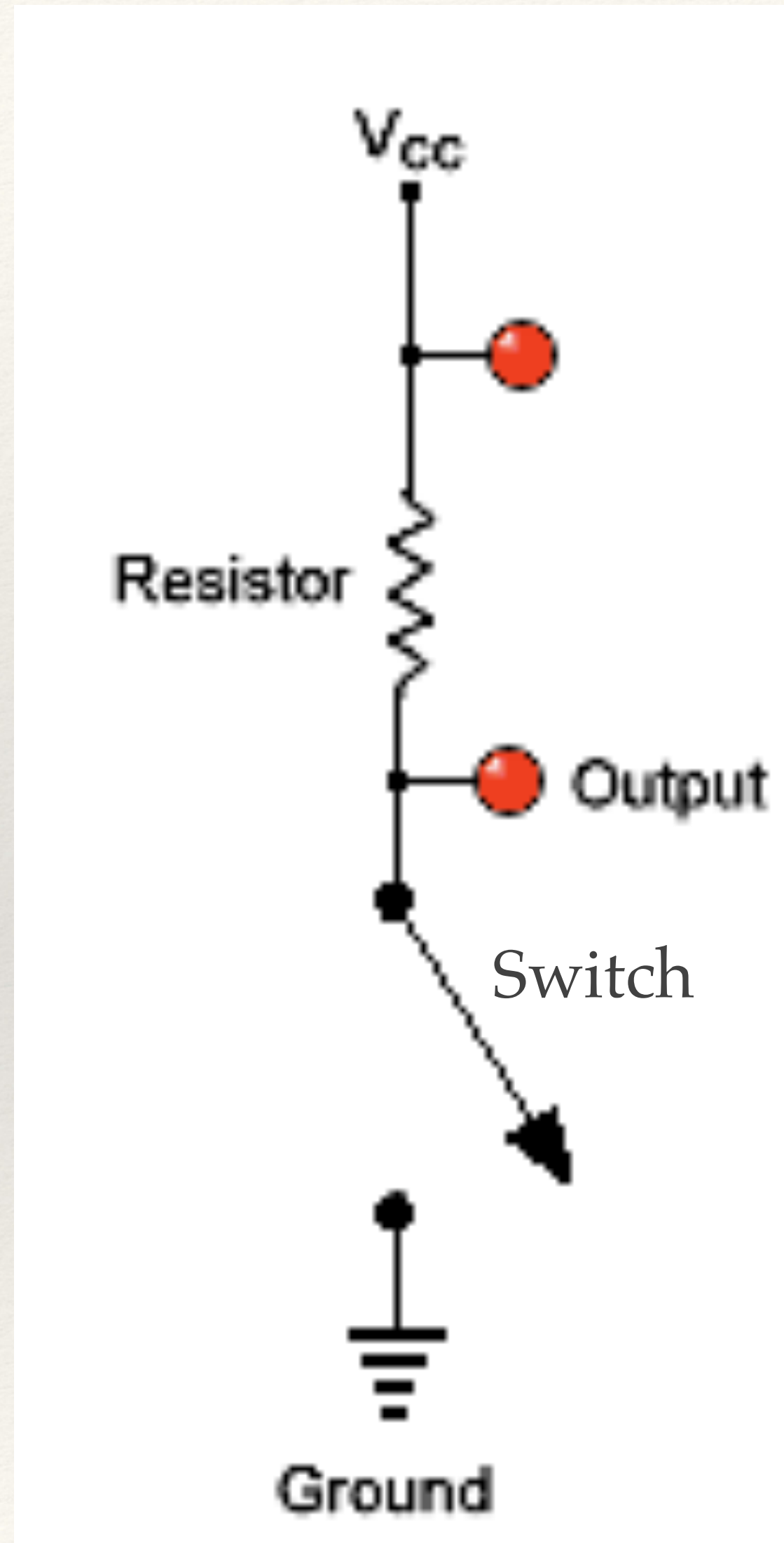
*When we remove the block, what is the effect on pressure?*

# The concept of pressure



*When we remove the block, what is the effect on pressure?*

# Electrical pressure: voltage



*If switch is off (0) (equivalent to the presence of the block)*

$$V_{\text{output}} = V_{cc} \text{ high (i.e. 1)}$$

*If switch is on (1) (equivalent to the absence of the block)*

$$V_{\text{output}} \ll V_{cc} \text{ low (i.e. 0)}$$

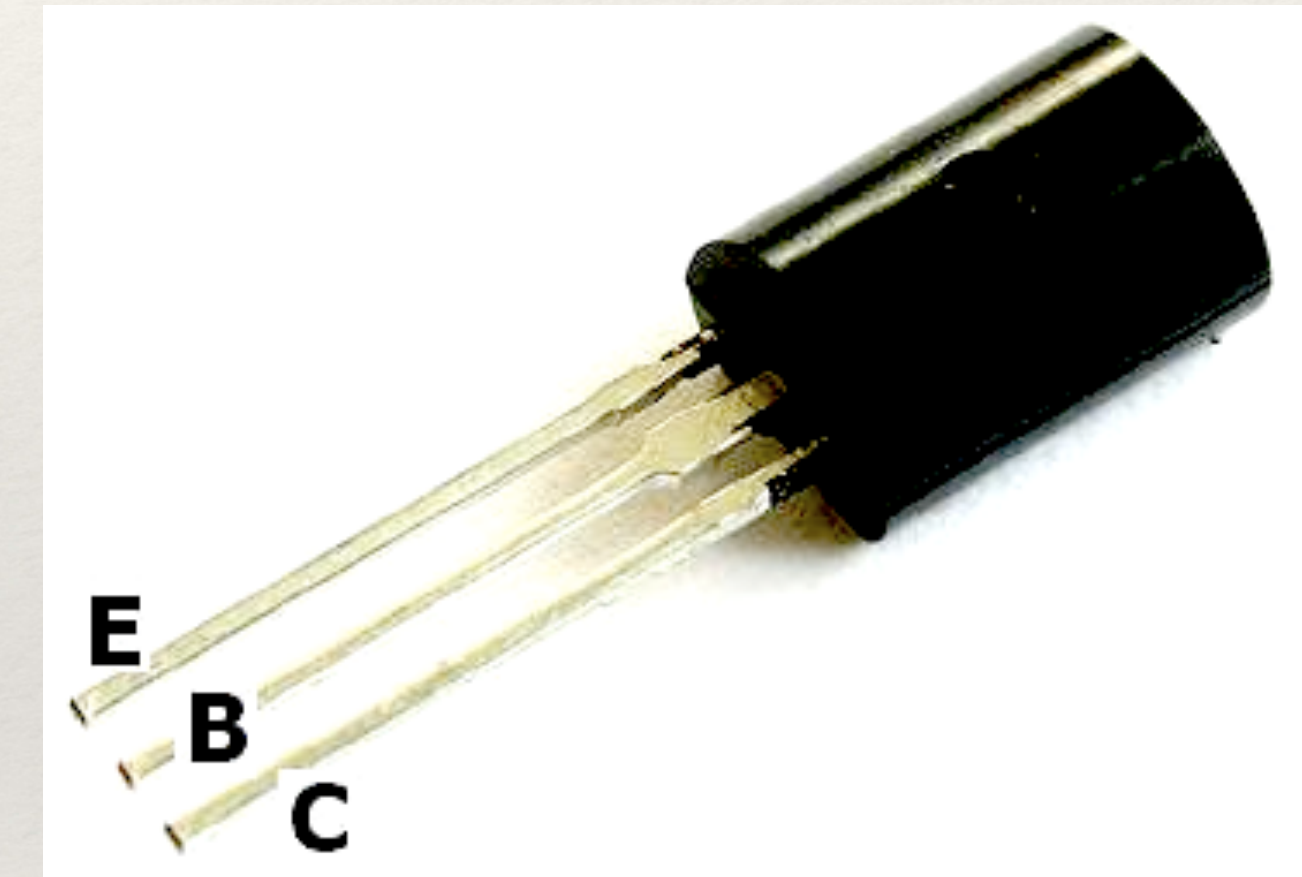
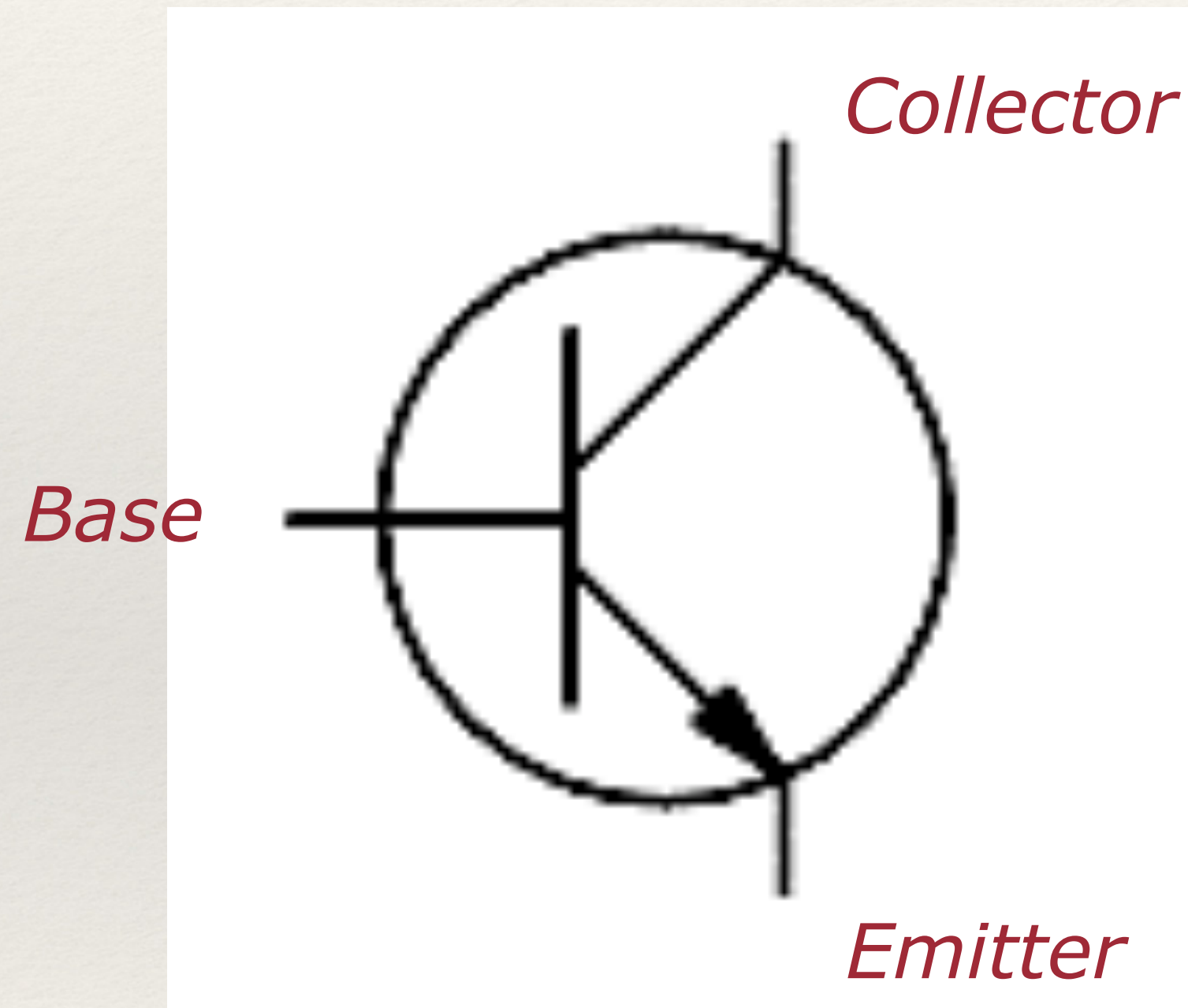
*"Inverter"*

# The transistor

A transistor can be used as an electronic switch:

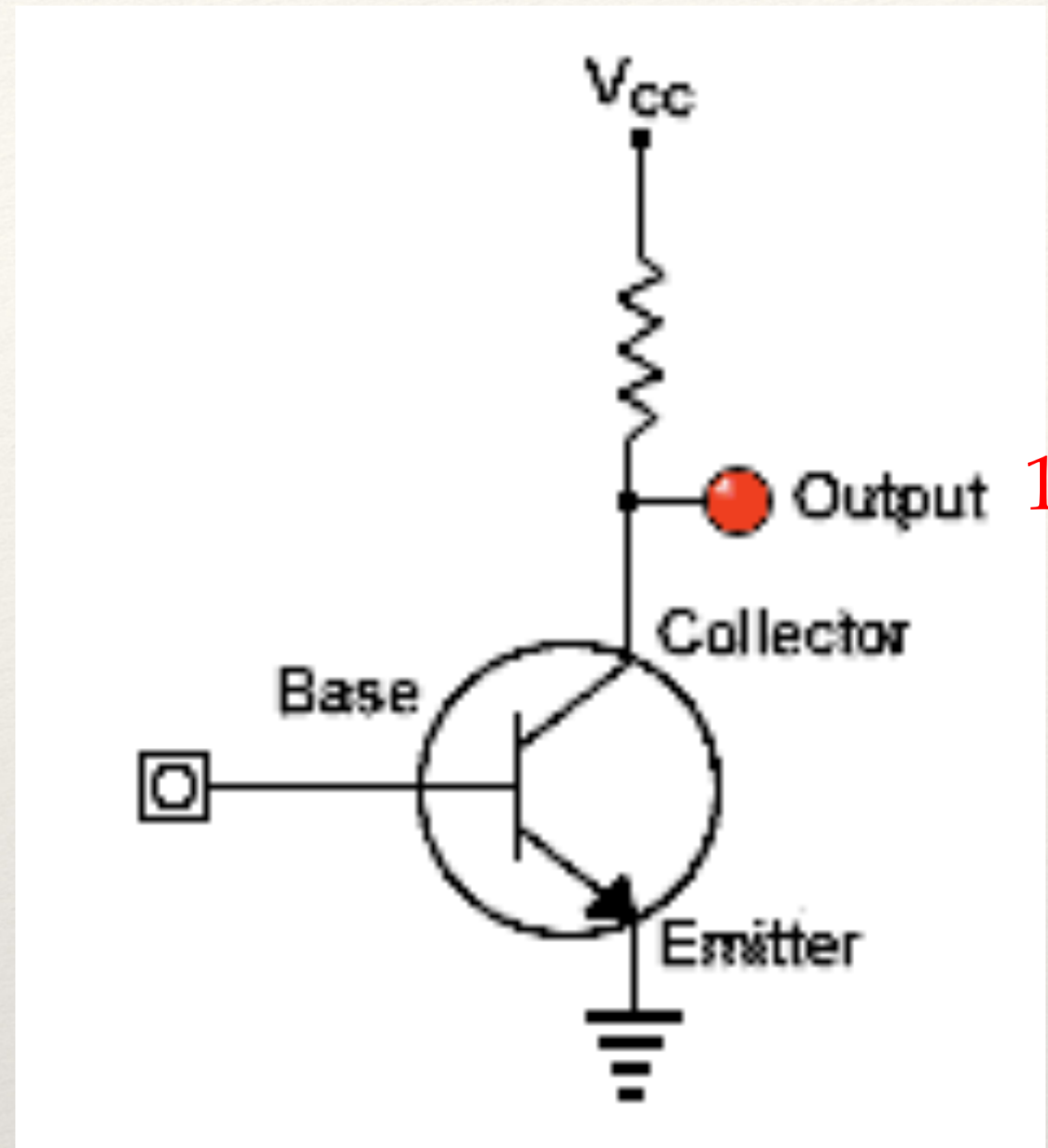
-if  $V_{\text{base}}$  is high, the current “flows” between the emitter and the collector  
(switch is on)

-If  $V_{\text{base}}$  is low, the current does not pass  
(switch is off)

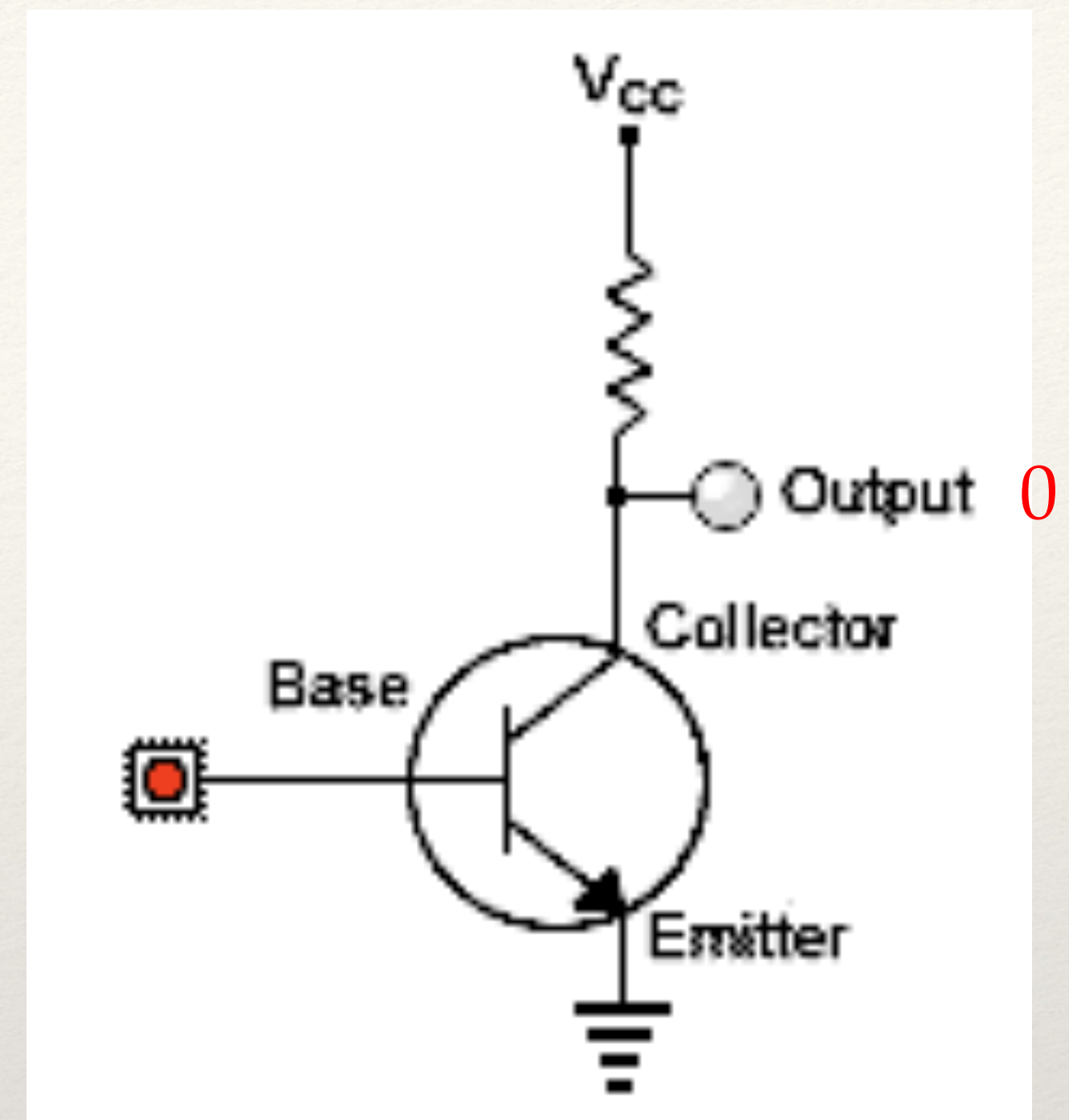


# The not gate

Input: 0



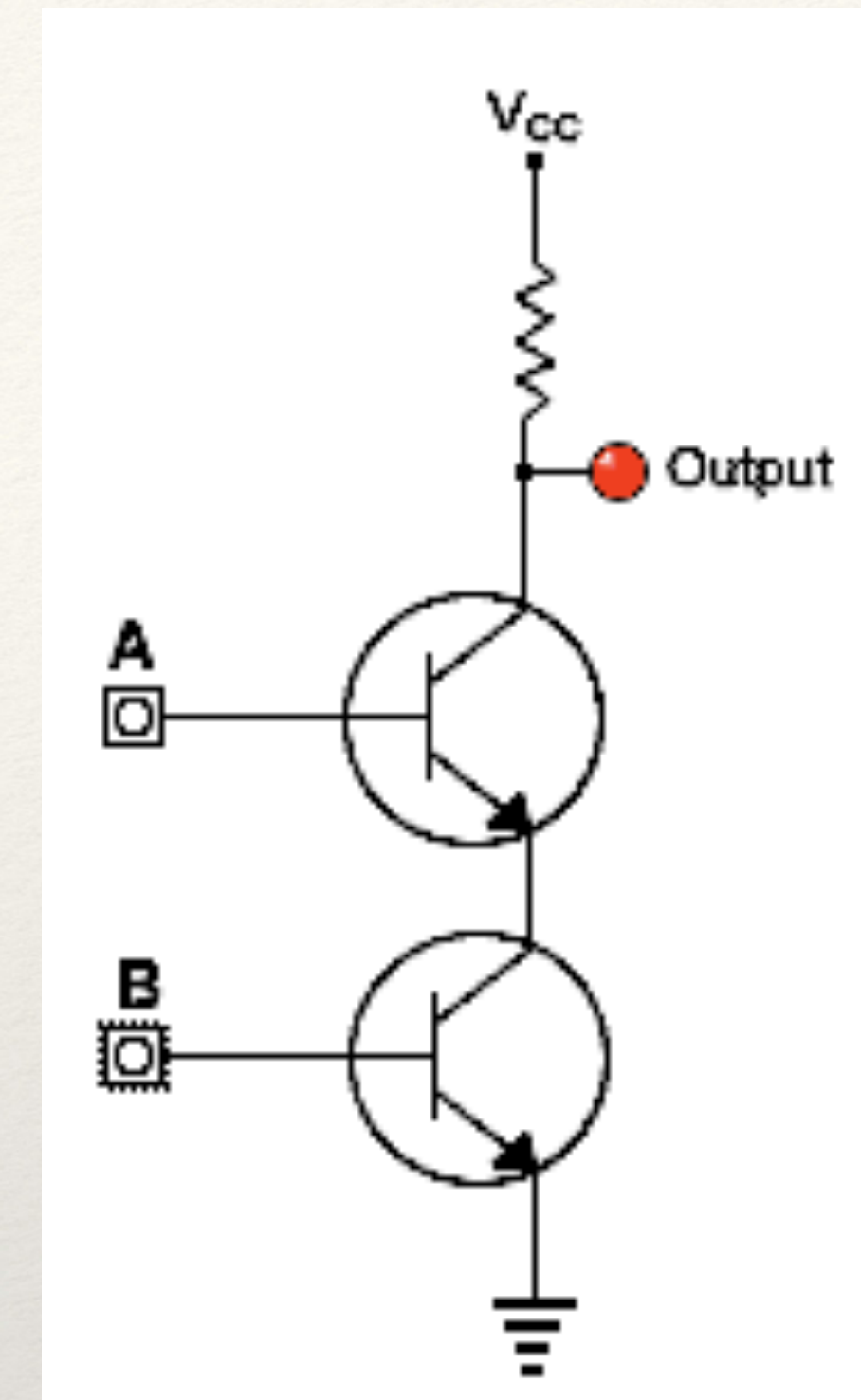
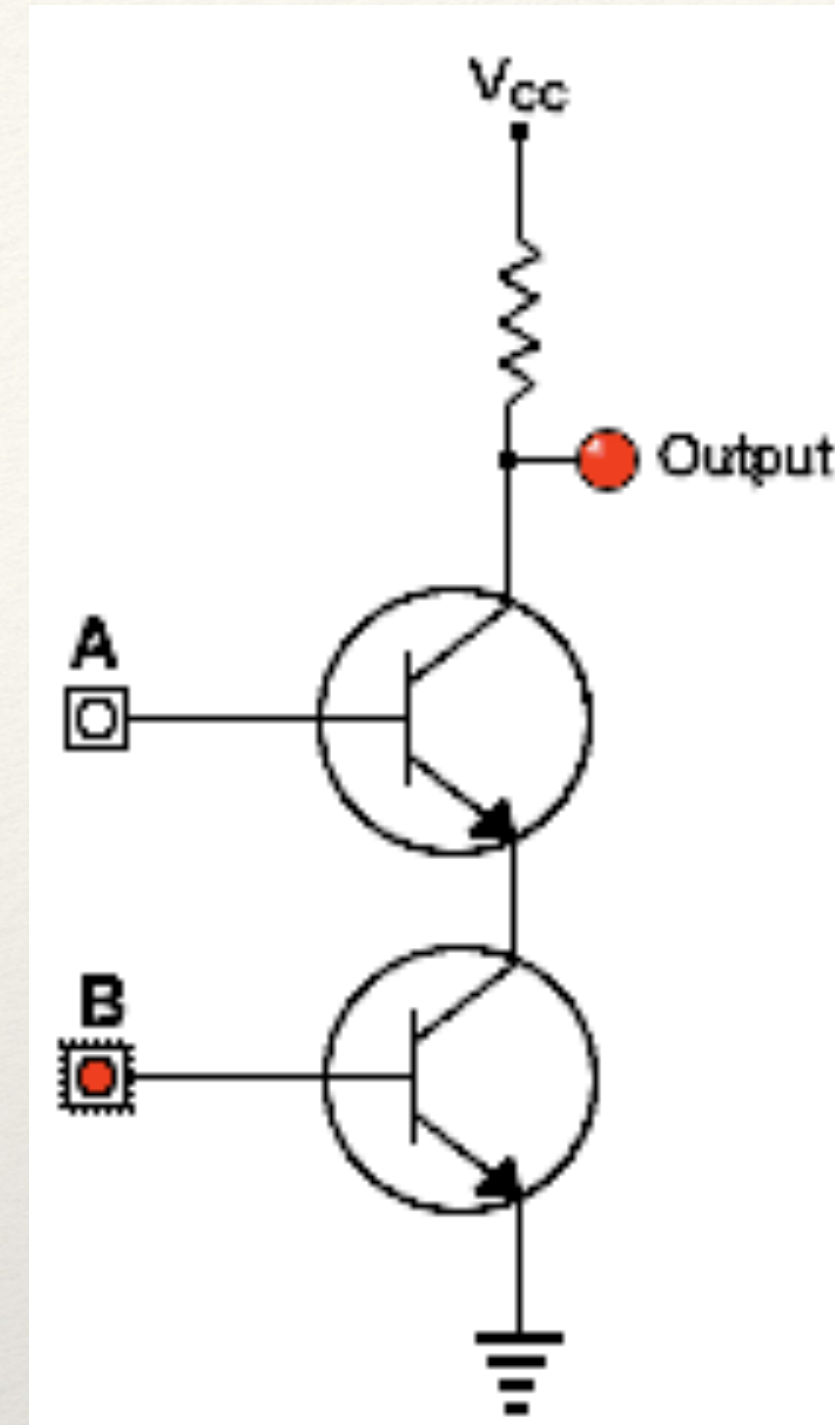
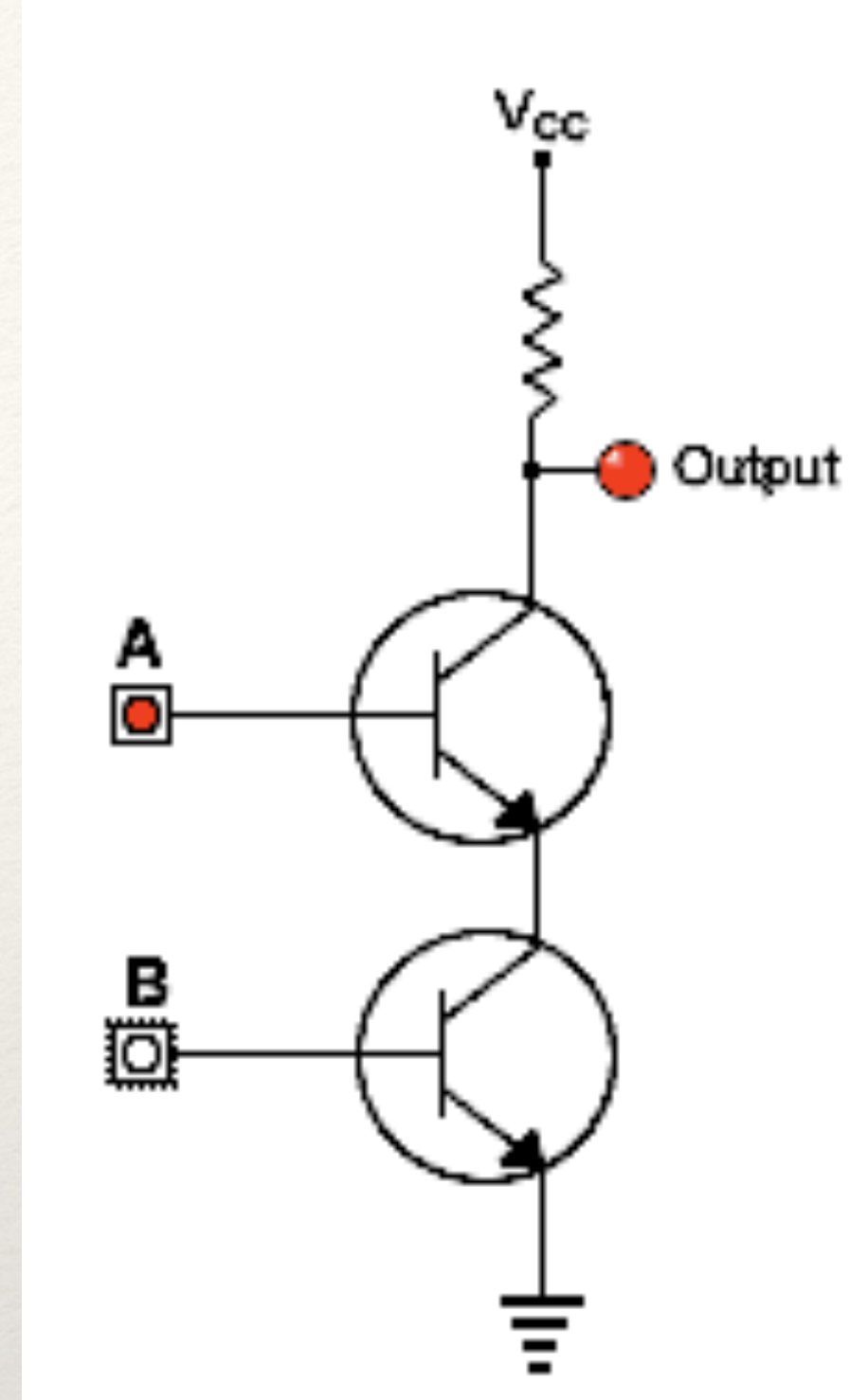
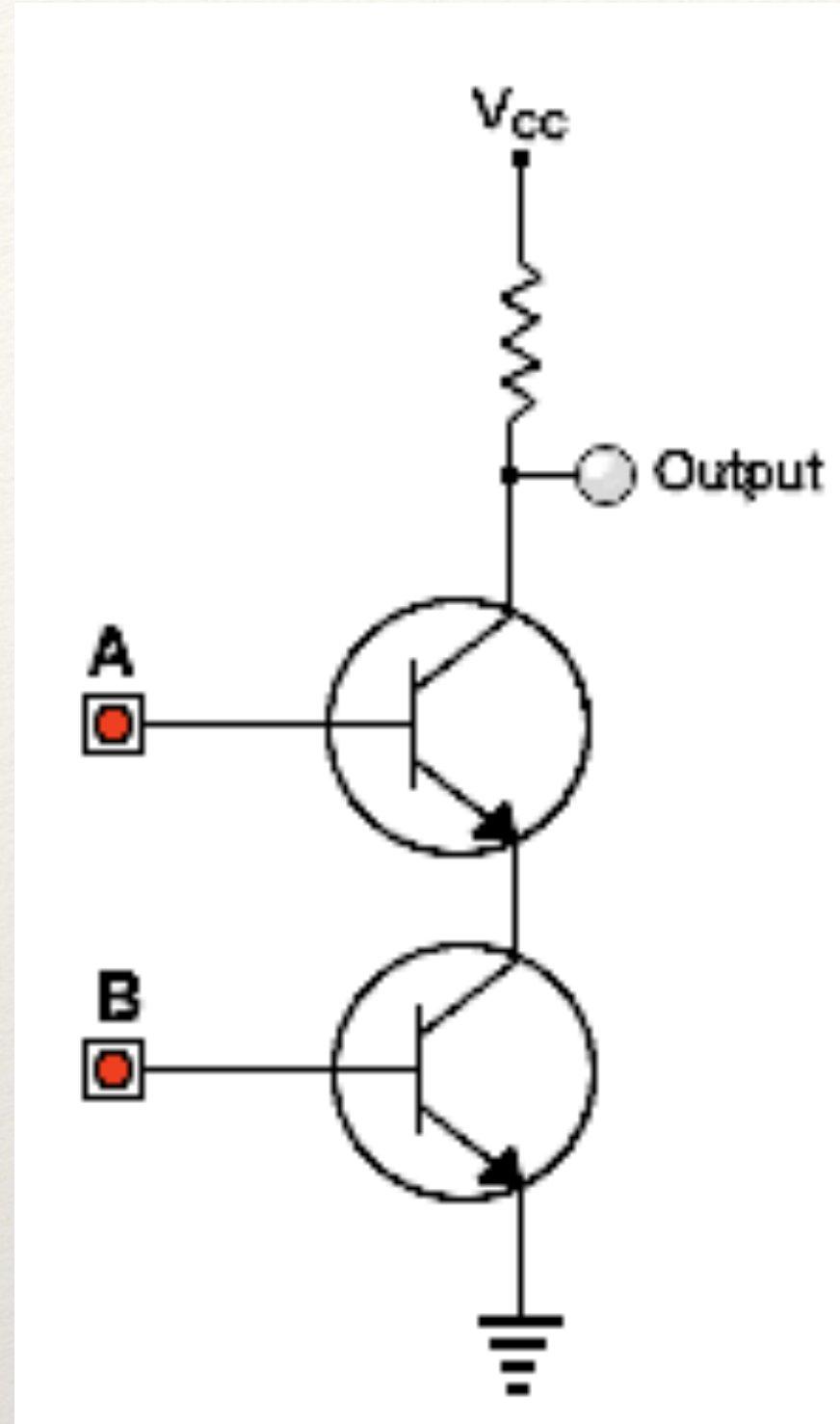
Input: 1



| Input | Output |
|-------|--------|
| 0     | 1      |
| 1     | 0      |

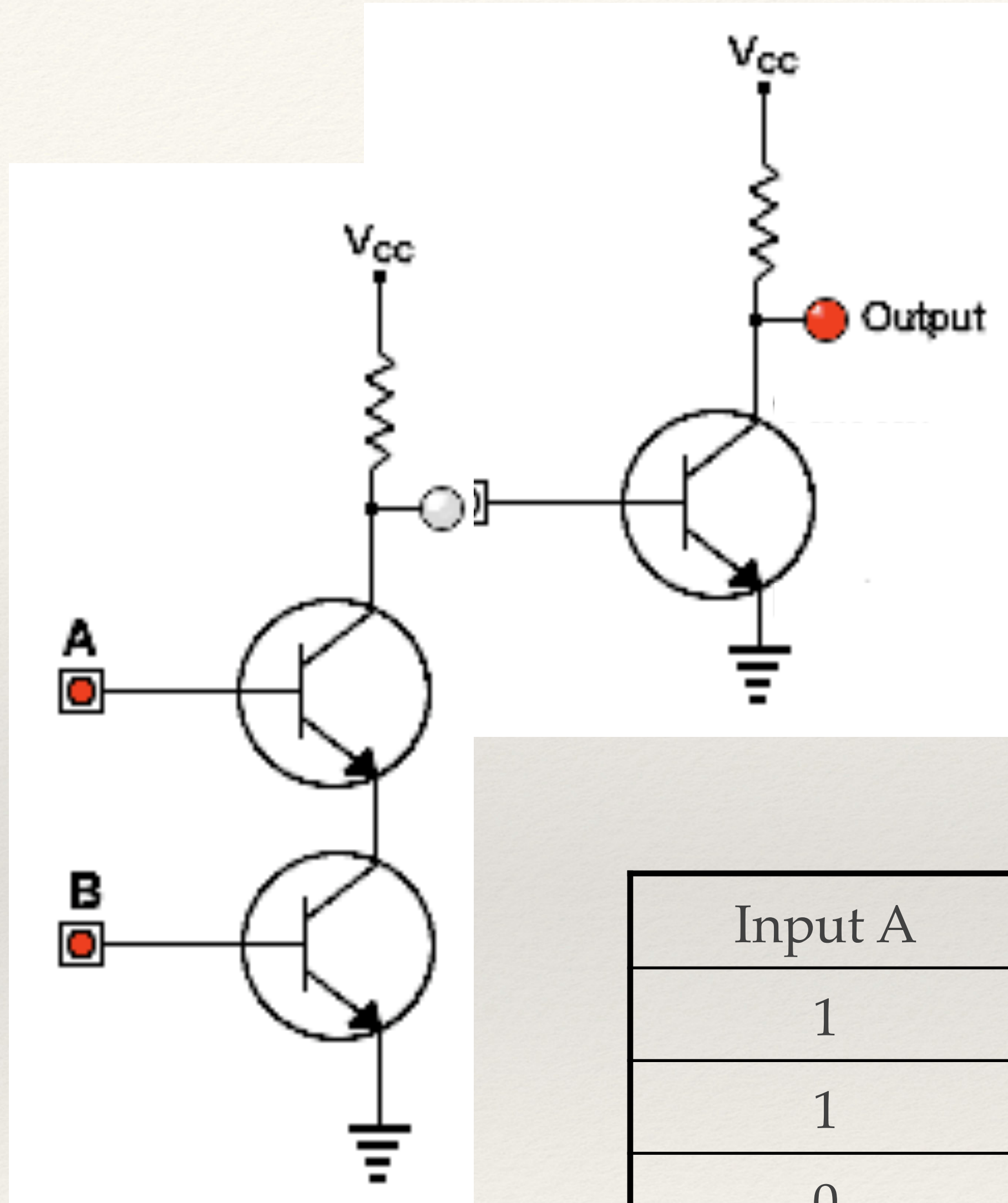


# The not-and (NAND) gate



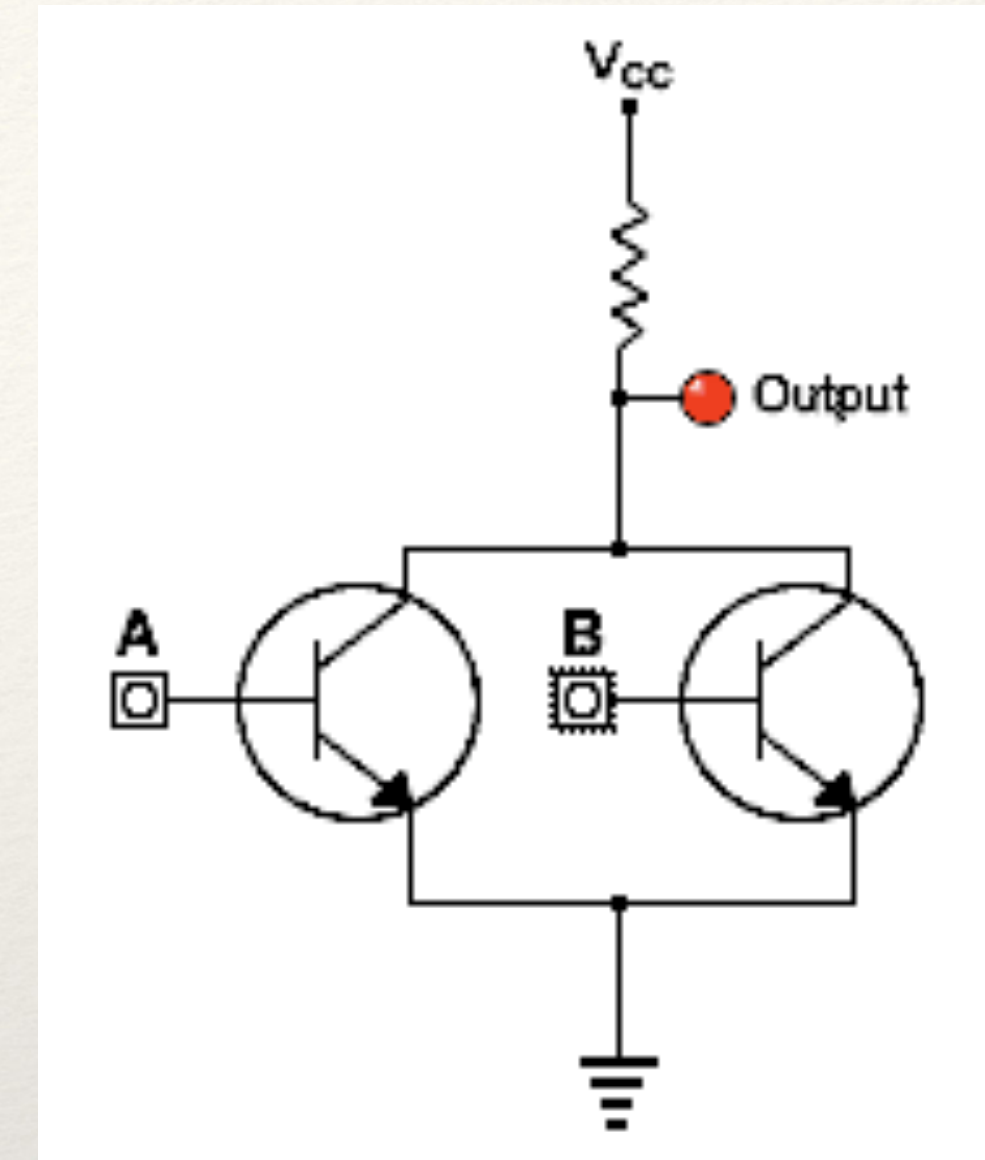
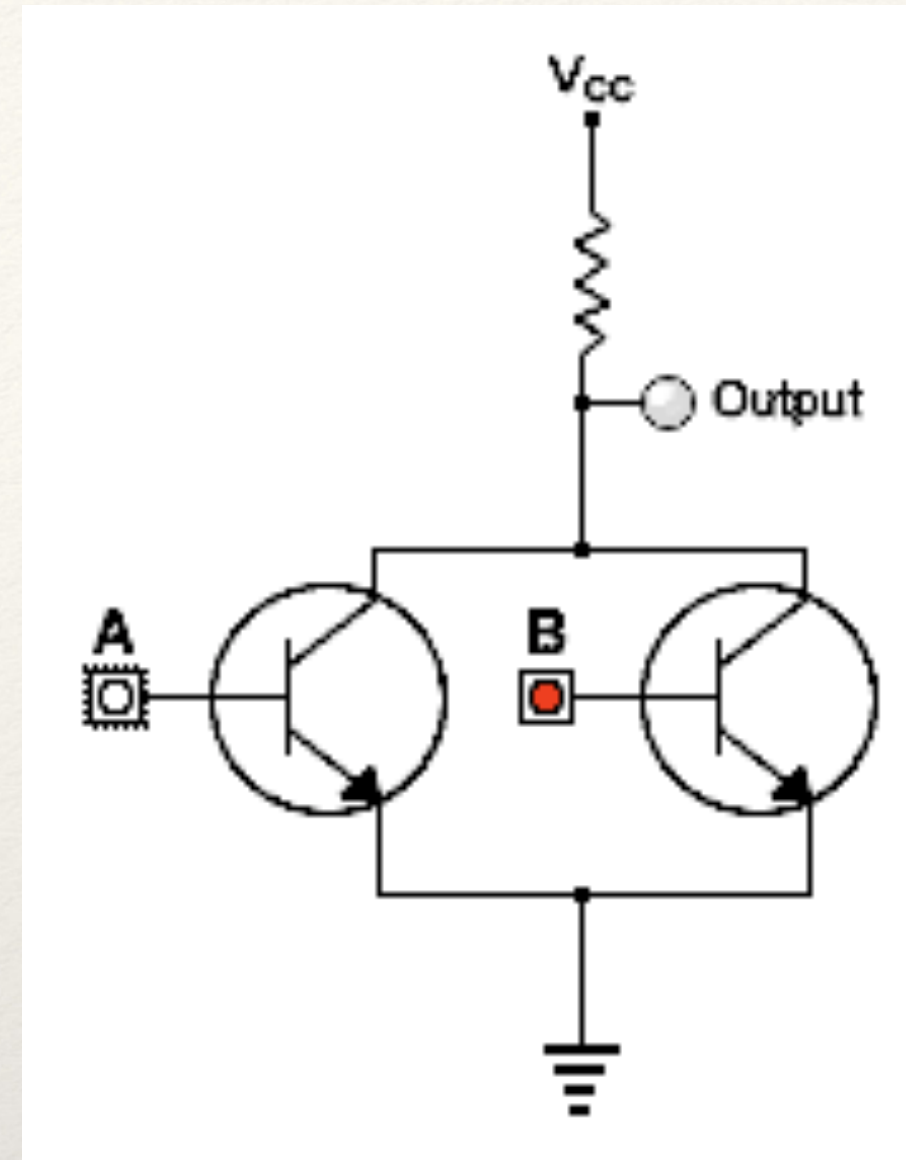
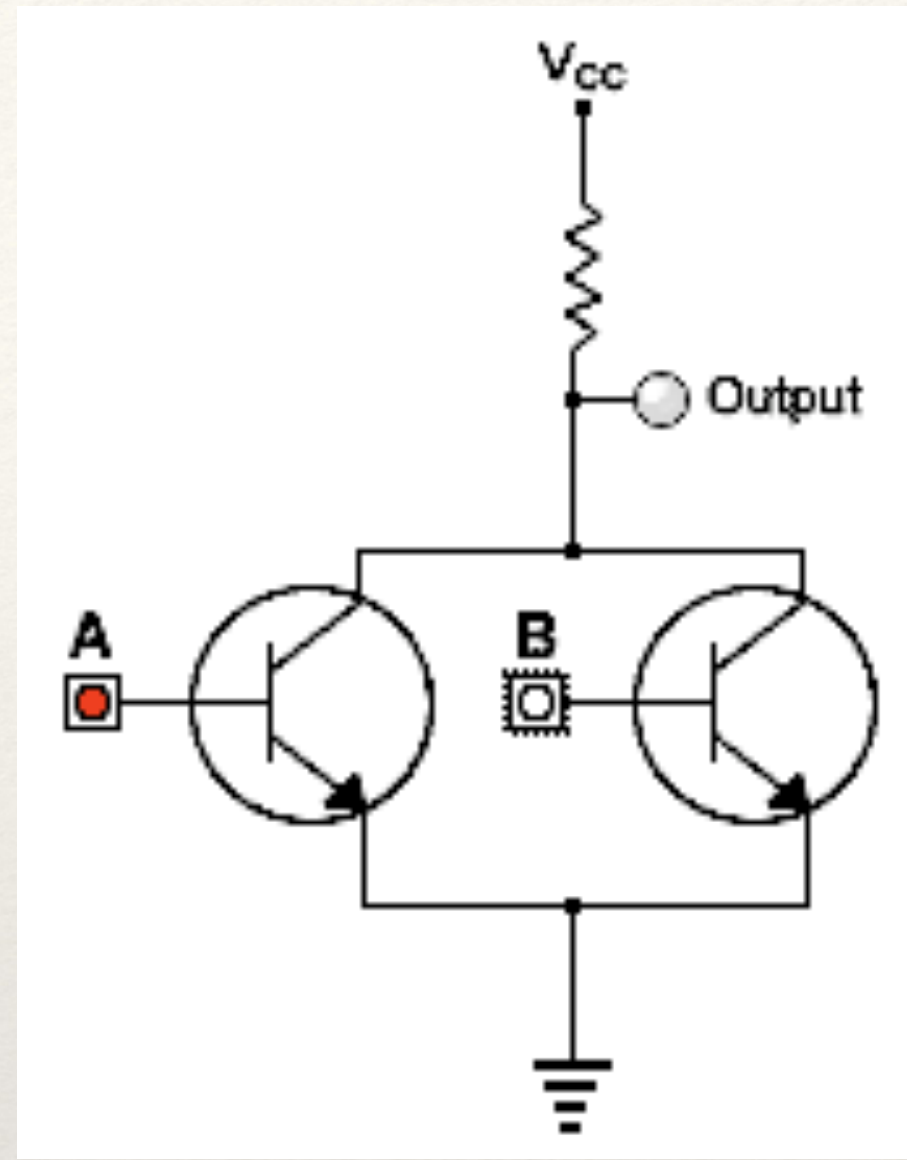
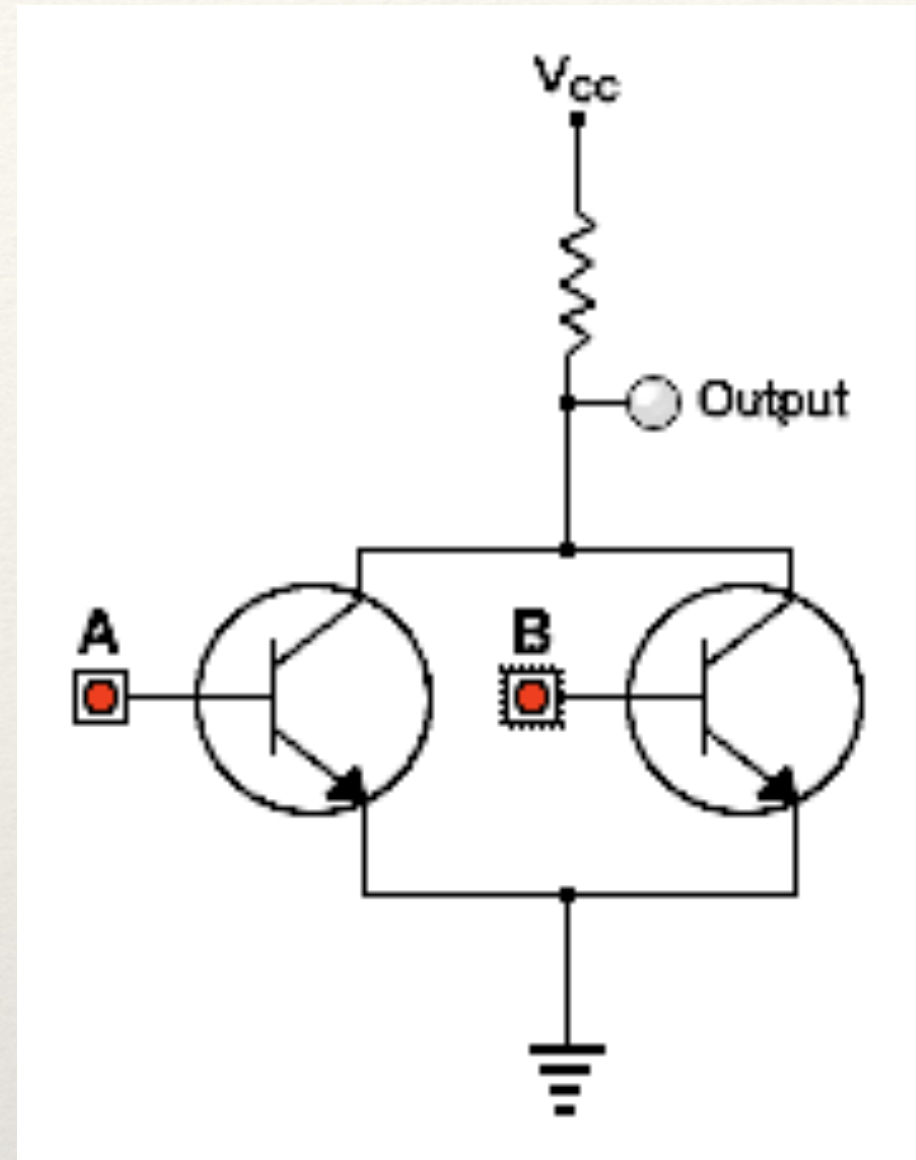
| Input A | Input B | Output |
|---------|---------|--------|
| 1       | 1       | 0      |
| 1       | 0       | 1      |
| 0       | 1       | 1      |
| 0       | 0       | 1      |

# The AND gate



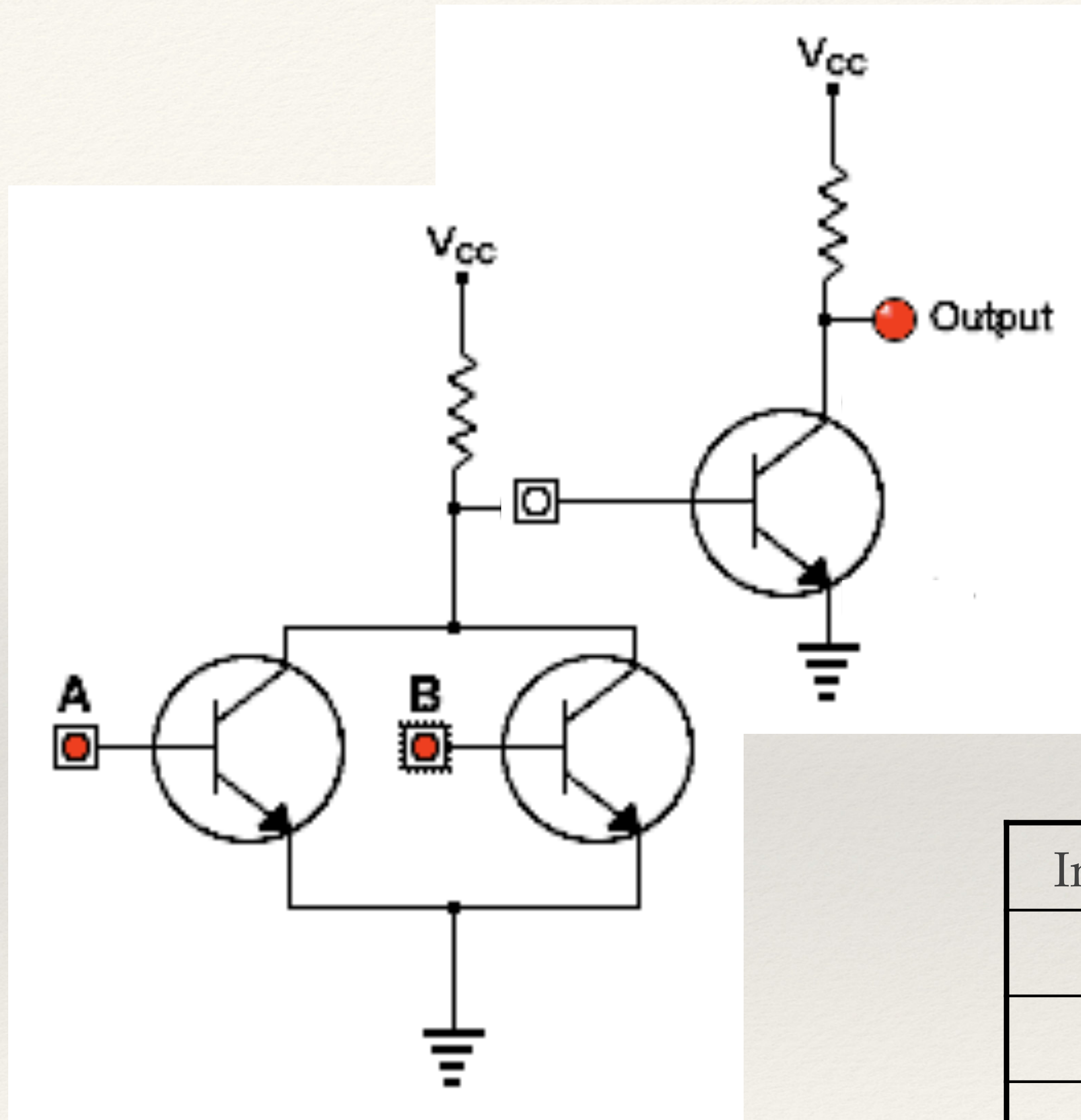
| Input A | Input B | Output |
|---------|---------|--------|
| 1       | 1       | 1      |
| 1       | 0       | 0      |
| 0       | 1       | 0      |
| 0       | 0       | 0      |

# The not-or (NOR) gate




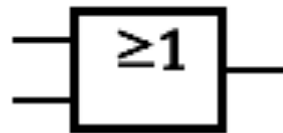

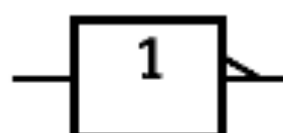

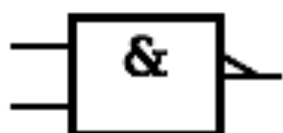

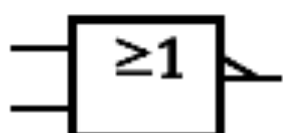


| Input A | Input B | Output |
|---------|---------|--------|
| 1       | 1       | 0      |
| 1       | 0       | 0      |
| 0       | 1       | 0      |
| 0       | 0       | 1      |

# The OR gate



| Input A | Input B | Output |
|---------|---------|--------|
| 1       | 1       | 1      |
| 1       | 0       | 1      |
| 0       | 1       | 1      |
| 0       | 0       | 0      |

| Type  | Distinctive shape   | Rectangular shape   | Boolean algebra between A & B | Truth table  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
|-------|---|---|-------------------------------|--|-------|--------|--------|-------|---|----------|---|---|---|---|---|---|---|---|---|---|---|---|
| AND   |    |    | $A \cdot B$                   | <table border="1"> <thead> <tr> <th colspan="2">INPUT</th> <th>OUTPUT</th> </tr> <tr> <th>A</th> <th>B</th> <th>A AND B</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>  | INPUT |        | OUTPUT | A     | B | A AND B  | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| INPUT |   | OUTPUT  |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| A     | B   | A AND B   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| 0     | 0   | 0   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| 0     | 1   | 0   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| 1     | 0   | 0   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| 1     | 1   | 1   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| OR    |    |    | $A + B$                       | <table border="1"> <thead> <tr> <th colspan="2">INPUT</th> <th>OUTPUT</th> </tr> <tr> <th>A</th> <th>B</th> <th>A OR B</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>   | INPUT |        | OUTPUT | A     | B | A OR B   | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| INPUT |   | OUTPUT  |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| A     | B   | A OR B  |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| 0     | 0   | 0   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| 0     | 1   | 1   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| 1     | 0   | 1   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| 1     | 1   | 1   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| NOT   |   |   | $\bar{A}$                     | <table border="1"> <thead> <tr> <th>INPUT</th> <th>OUTPUT</th> </tr> <tr> <th>A</th> <th>NOT A</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> </tr> </tbody> </table>   | INPUT | OUTPUT | A      | NOT A | 0 | 1        | 1 | 0 |   |   |   |   |   |   |   |   |   |   |
| INPUT | OUTPUT  |   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| A     | NOT A   |   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| 0     | 1   |   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| 1     | 0   |   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| NAND  |  |  | $\overline{A \cdot B}$        | <table border="1"> <thead> <tr> <th colspan="2">INPUT</th> <th>OUTPUT</th> </tr> <tr> <th>A</th> <th>B</th> <th>A NAND B</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table> | INPUT |        | OUTPUT | A     | B | A NAND B | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| INPUT |   | OUTPUT  |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| A     | B   | A NAND B  |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| 0     | 0   | 1   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| 0     | 1   | 1   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| 1     | 0   | 1   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| 1     | 1   | 0   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| NOR   |  |  | $\overline{A + B}$            | <table border="1"> <thead> <tr> <th colspan="2">INPUT</th> <th>OUTPUT</th> </tr> <tr> <th>A</th> <th>B</th> <th>A NOR B</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>  | INPUT |        | OUTPUT | A     | B | A NOR B  | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| INPUT |   | OUTPUT  |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| A     | B   | A NOR B   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| 0     | 0   | 1   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| 0     | 1   | 0   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| 1     | 0   | 0   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |
| 1     | 1   | 0   |                               |  |       |        |        |       |   |          |   |   |   |   |   |   |   |   |   |   |   |   |

# Computers

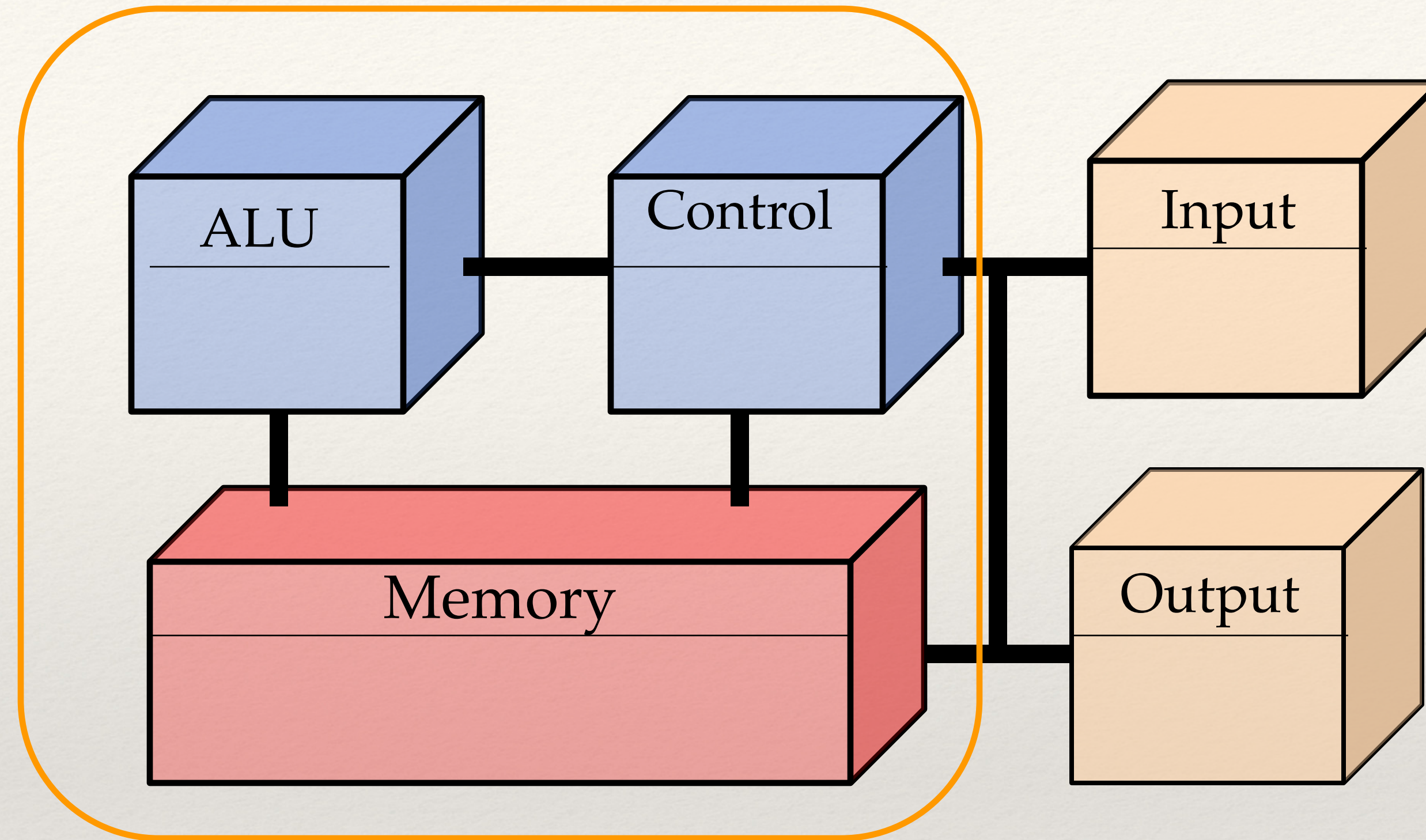
Logic: acting on information

The Central Processing Unit (CPU)

Elements of a Computer

# The Central Process Unit (CPU)

*CPU*



*The CPU consists of three parts:*  
the Arithmetic Logic Unit (ALU)  
The Control Unit  
Memory

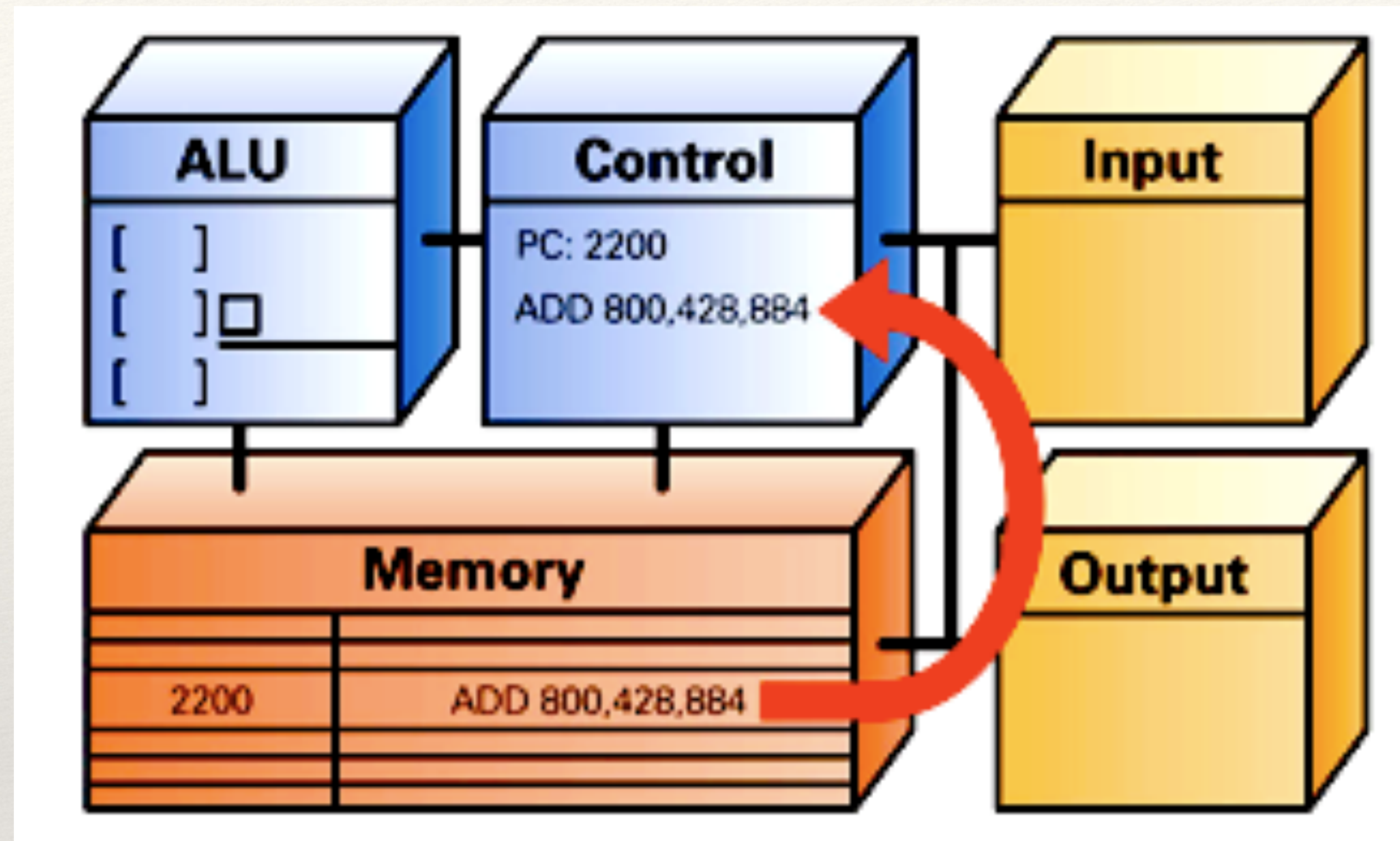
# The Fetch / Execute Cycle

The CPU cycles through a series of operations or instructions, organized in a cycle, the Fetch / Execute cycle:

1. Instruction Fetch (IF)
2. Instruction Decode (DP)
3. Data Fetch (DF)
4. Instruction Execute (IE)
5. Result Return



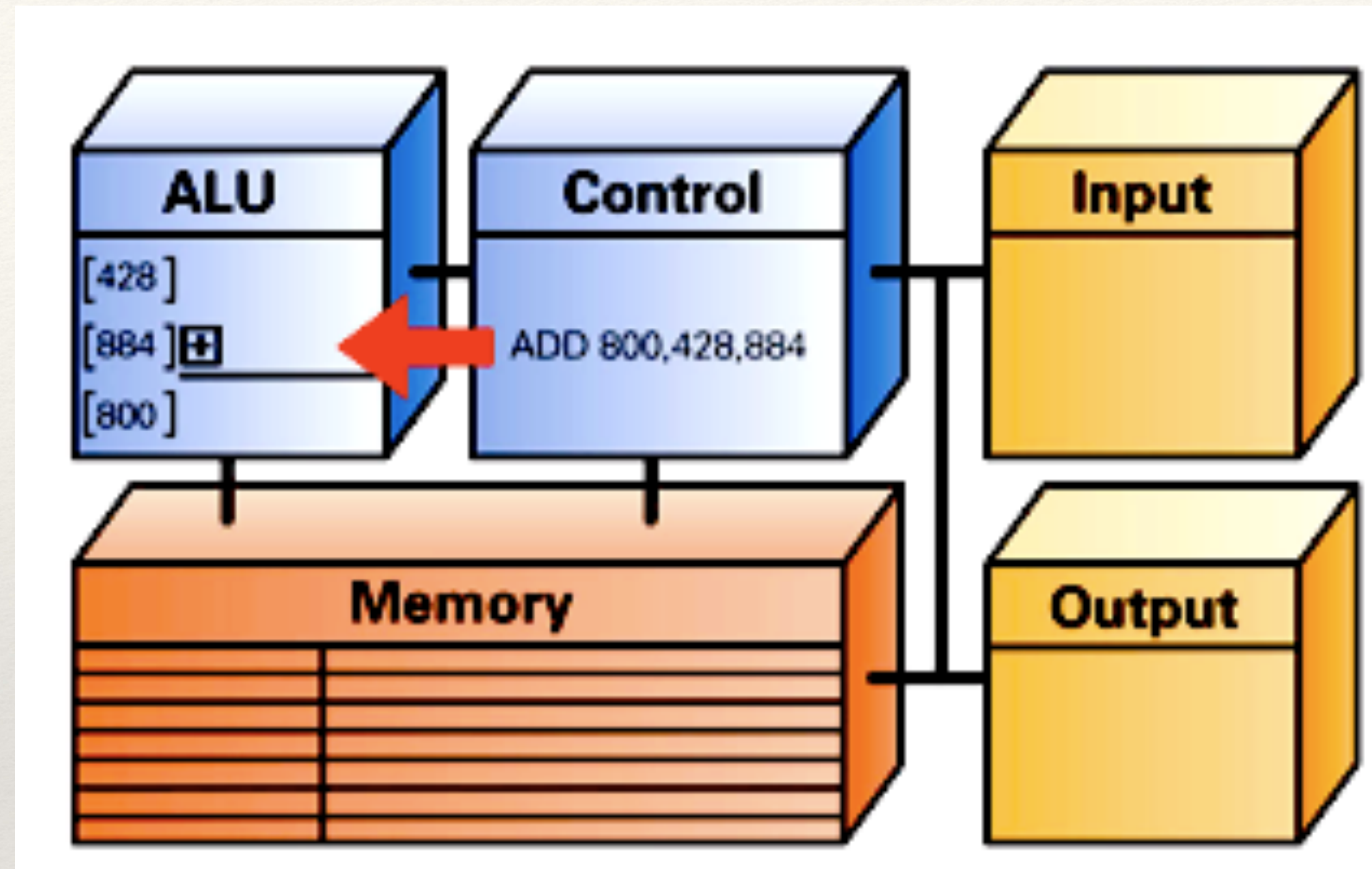
# Step 1: Instruction Fetch



Fetch instruction from memory position 2200:

Add numbers in memory positions 884 and 428, and store results at position 800

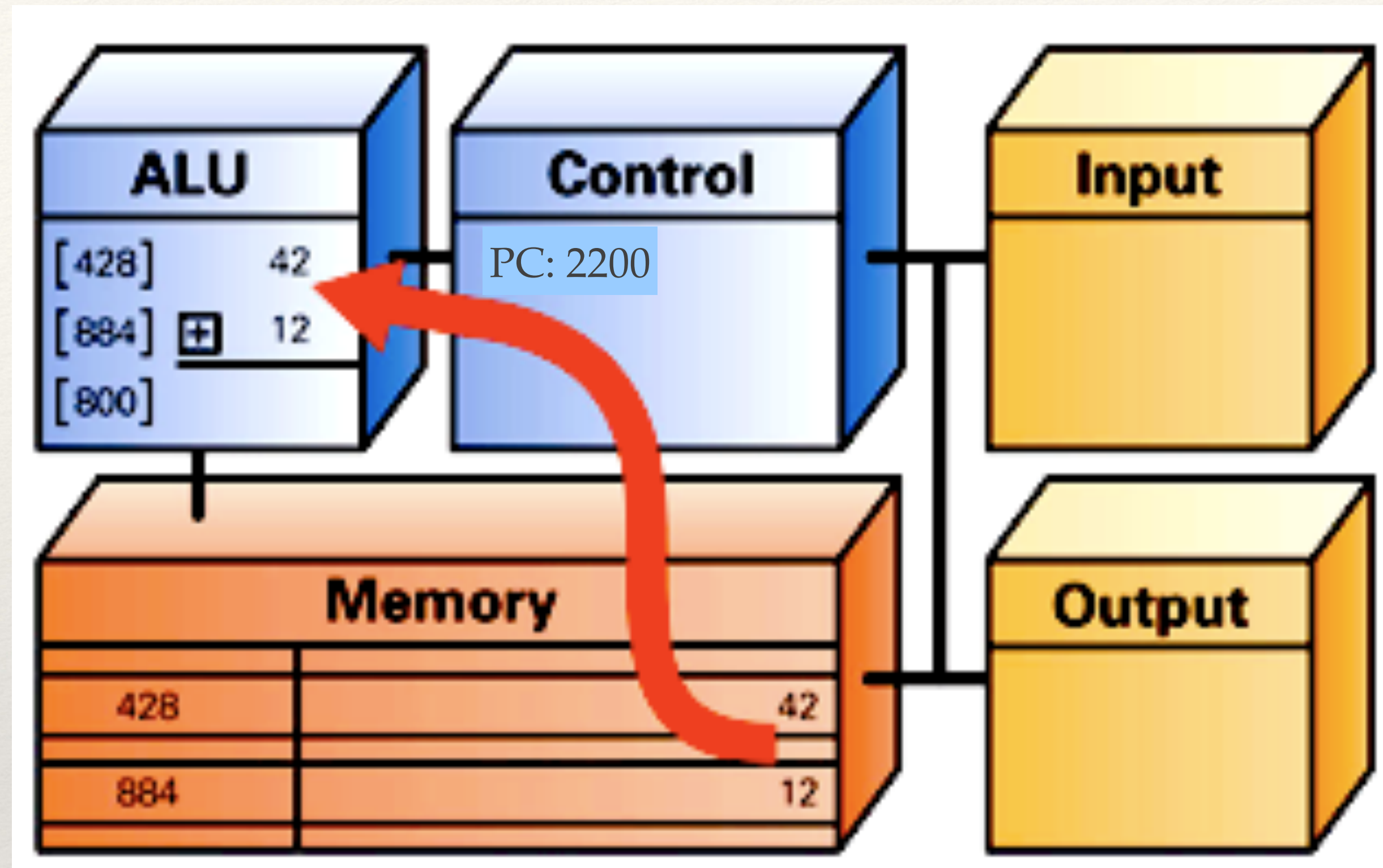
## Step 2: Instruction Decode



Decode instruction:

Defines operation (+), and set memory pointers in ALU

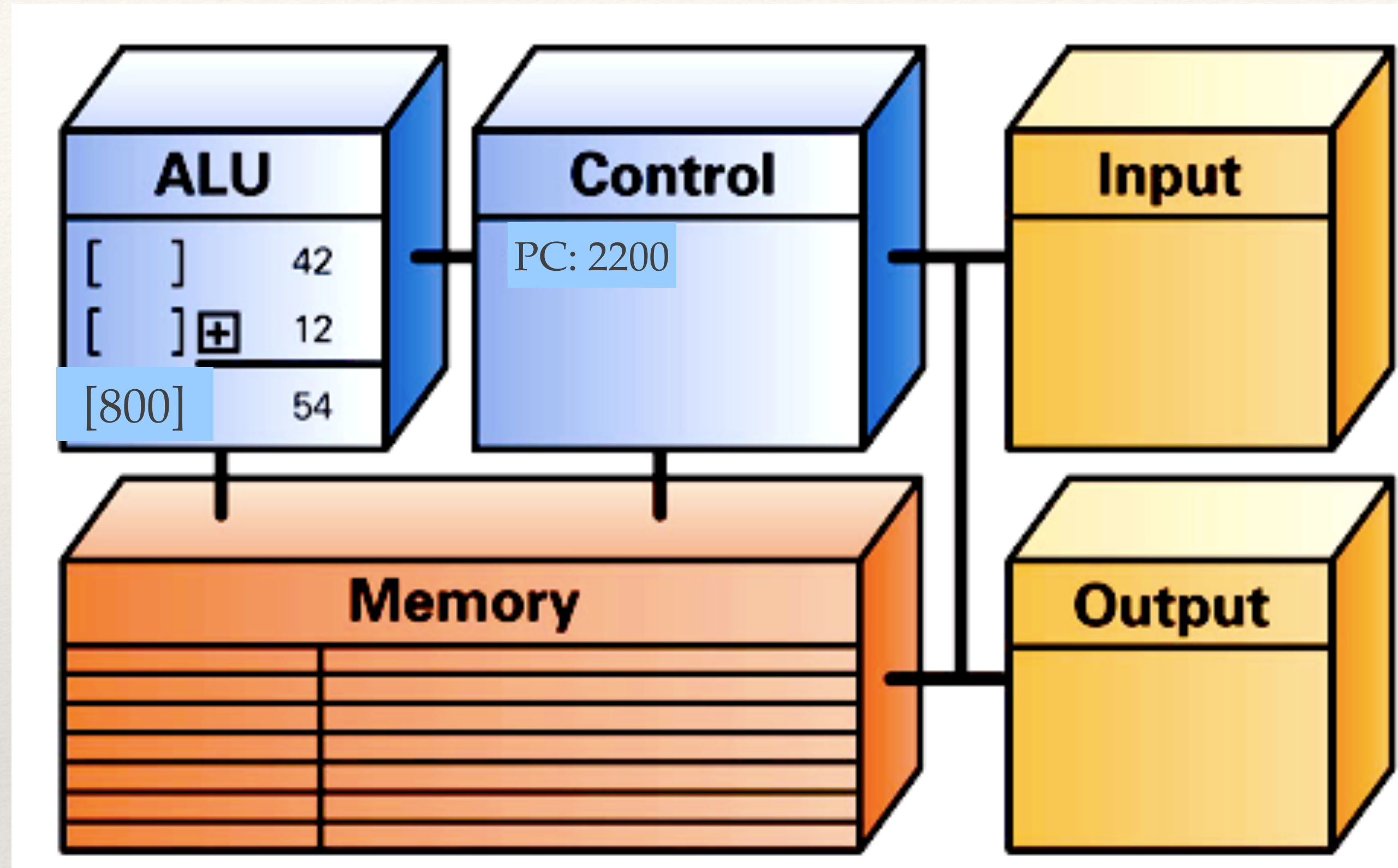
# Step 3: Data Fetch



Fetch data:

Get numbers at memory positions 428 and 884: 42 and 12  
and put in ALU

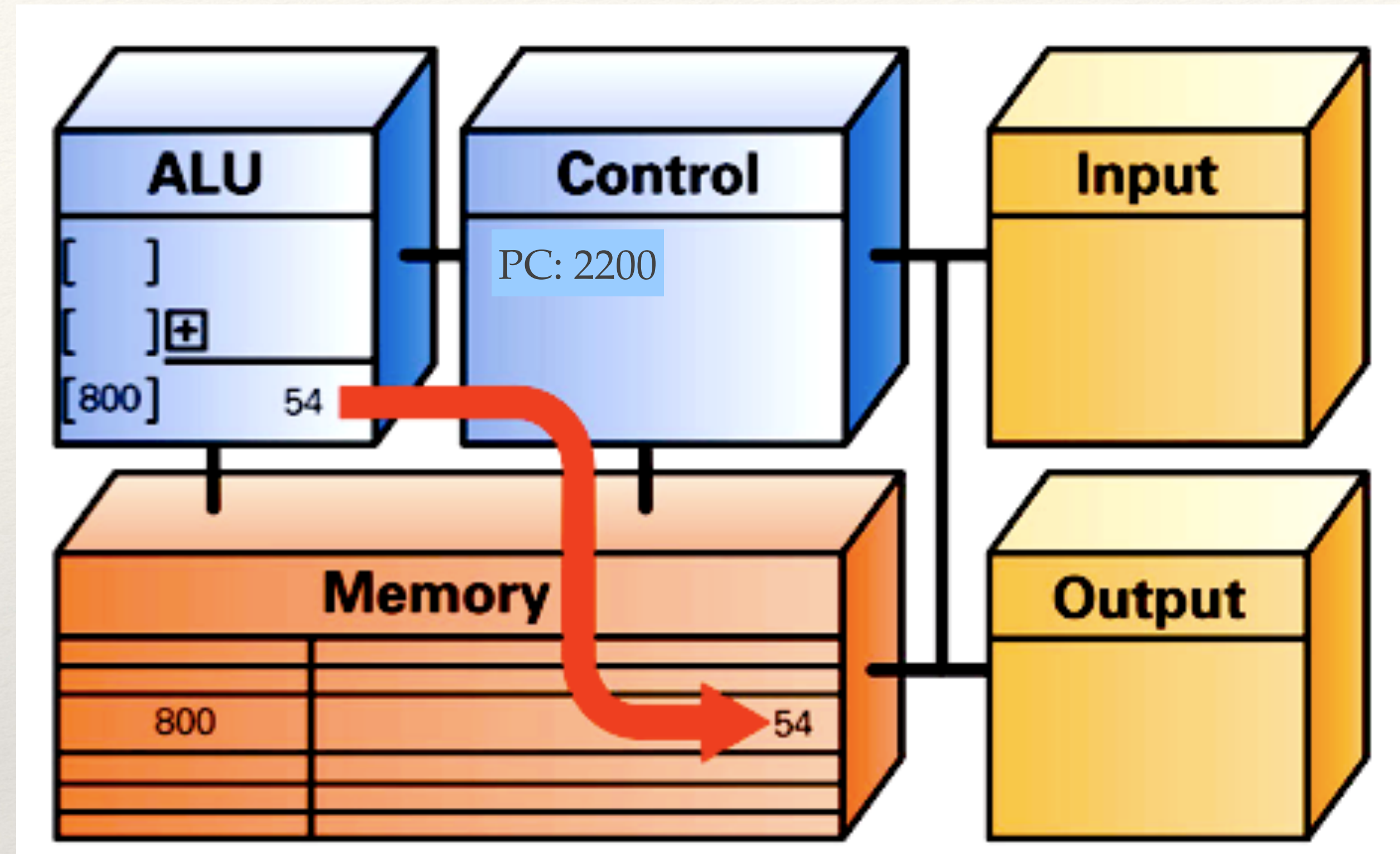
# Step 4: Instruction Execution



Execute:

Add numbers 42 and 12 in ALU: 54

# Step 5: Return Result



Return:

Put results (54) in position 800 in memory

# Possible operations

Computers can only perform about 100 different types of operations; all other operations must be broken down into simpler operations among these 100.

*Some of these operations:*

- Add, Mult, Div
- AND, OR, NAND, NOR, ...
- Bit shifts
- Test if a bit is 0 or 1
- Move information in memory
- ...

# Repeating the F / E cycle

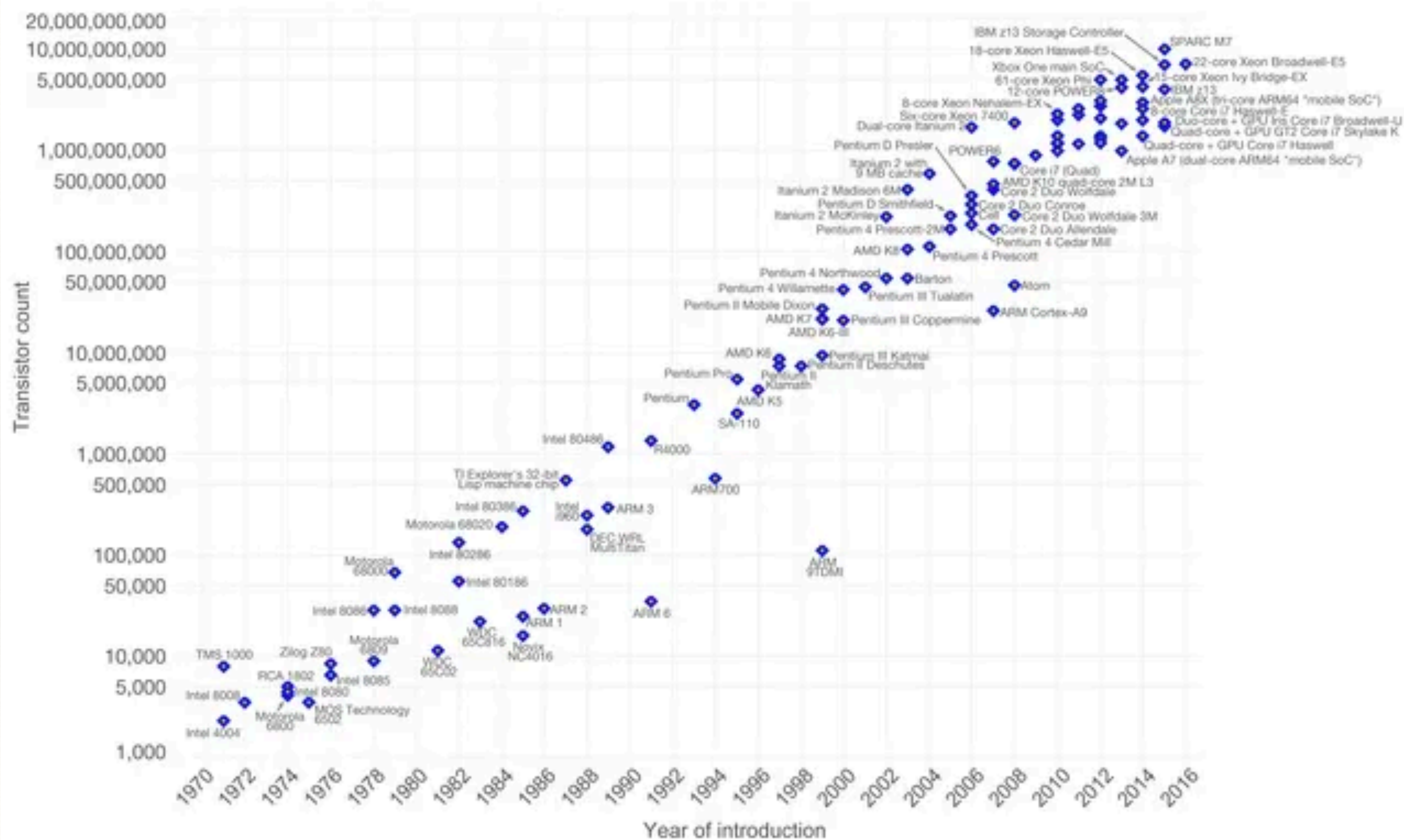
Computers get their impressive capabilities by performing many of these F / E cycles per second.

The **computer clock** determines the rate of F / E cycles per second; it is now expressed in GHz, i.e. in billions of cycles per seconds!

*Note that the rate given is not an exact measurement.*

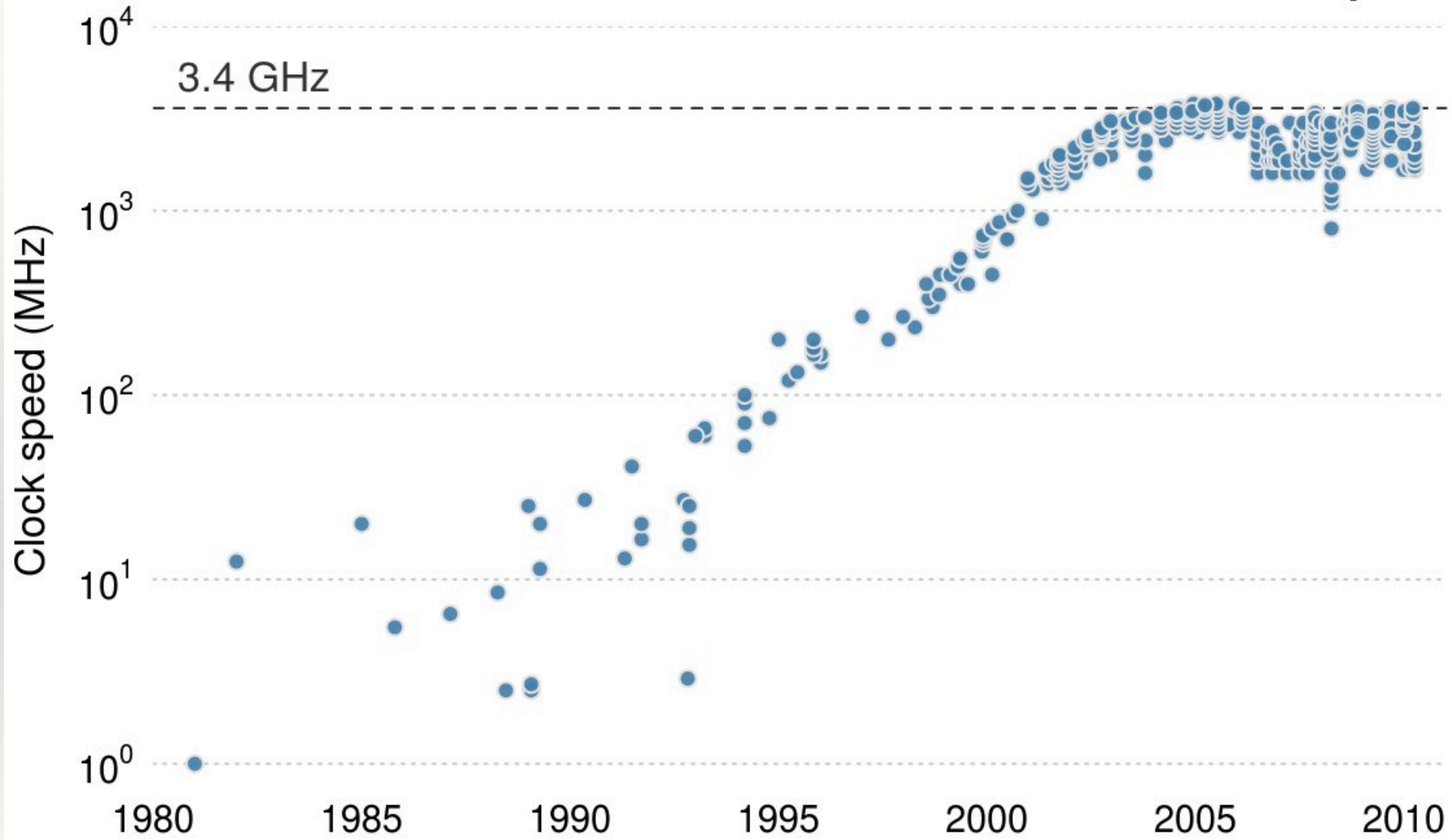
# Moore's Law – The number of transistors on integrated circuit chips (1971-2016)

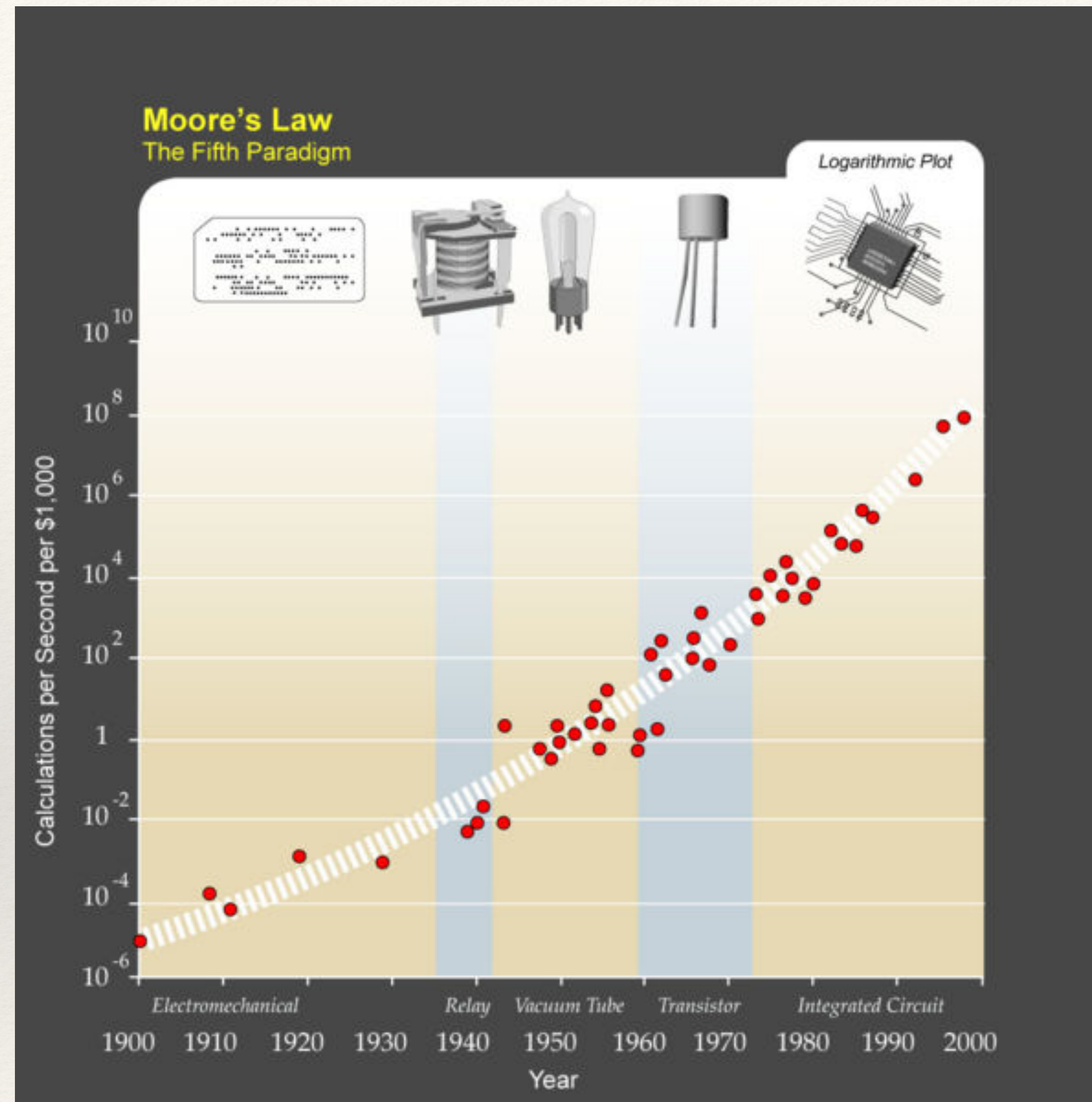
Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are strongly linked to Moore's law.





# CPU Clock Speed

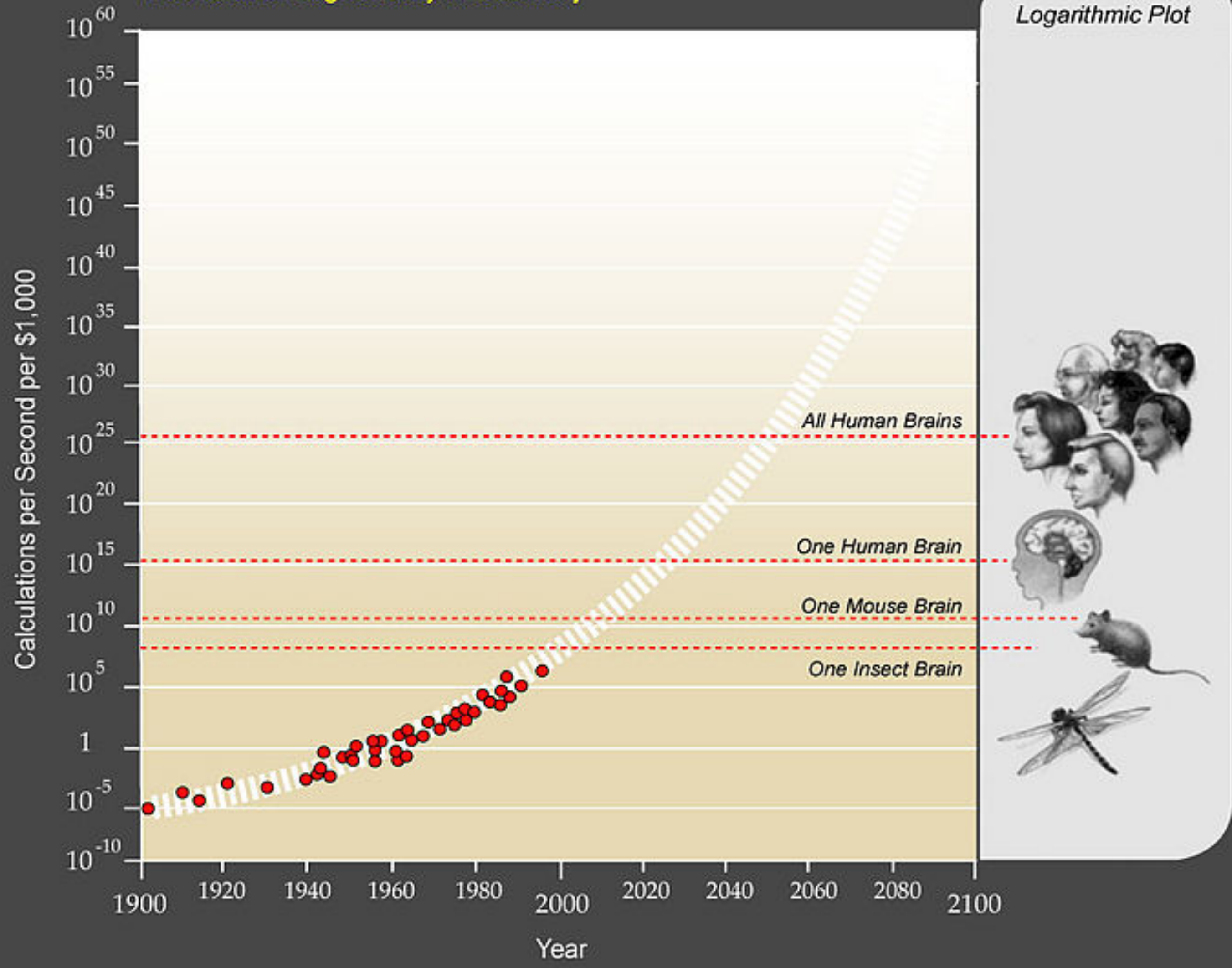




([http://en.wikipedia.org/wiki/Accelerating\\_change](http://en.wikipedia.org/wiki/Accelerating_change))

# Exponential Growth of Computing

Twentieth through twenty first century



([http://en.wikipedia.org/wiki/Accelerating\\_change](http://en.wikipedia.org/wiki/Accelerating_change))

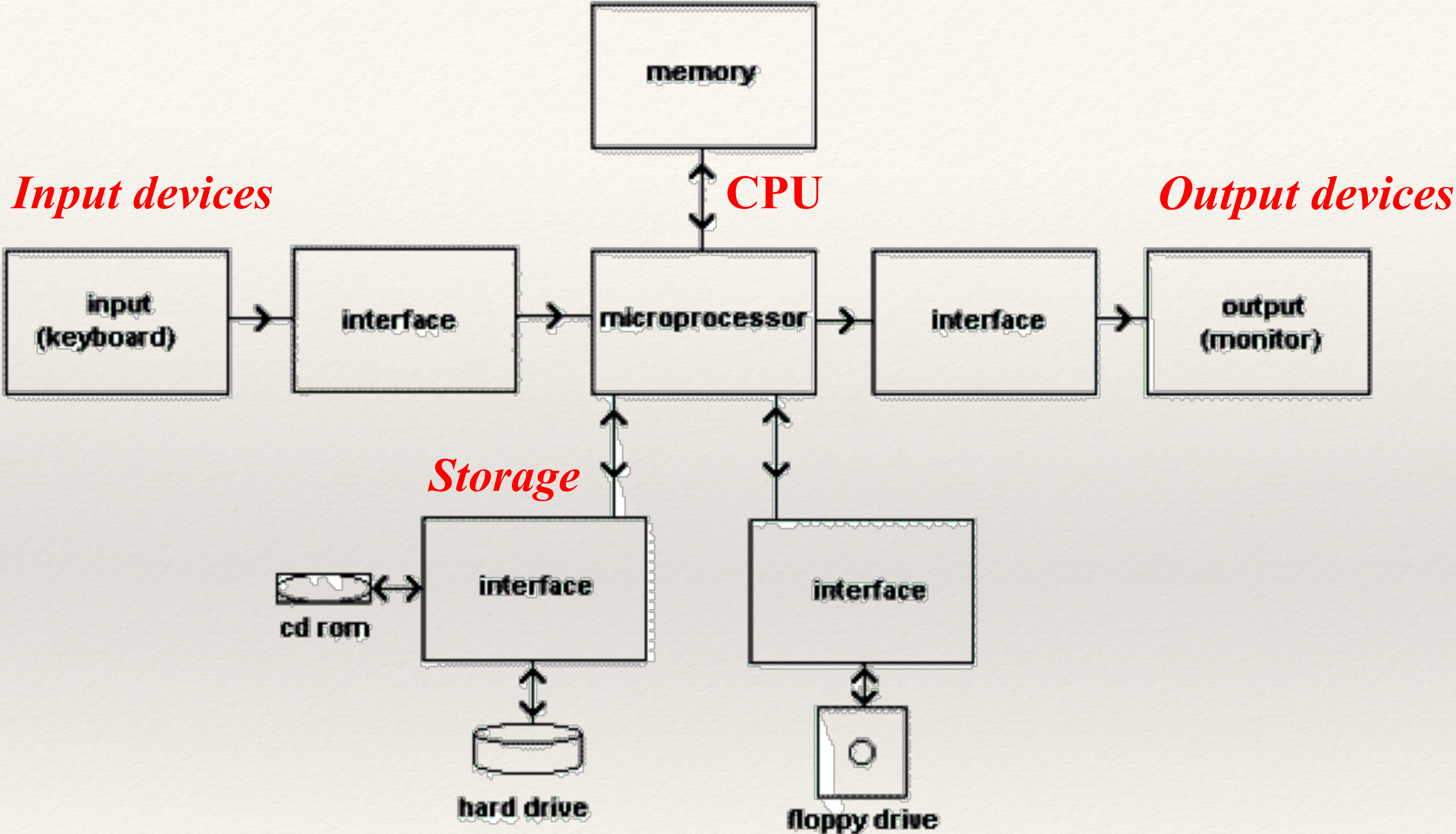
# Computers

Logic: acting on information

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Elements of a Computer

# Computer: basic scheme



# The Central Process Unit (CPU)



CPUs are getting smaller, and can include more than one “core” (or processors).



CPUs get hot, as their internal components dissipate heat: it is important to add a heat sink and fans to keep them cool.

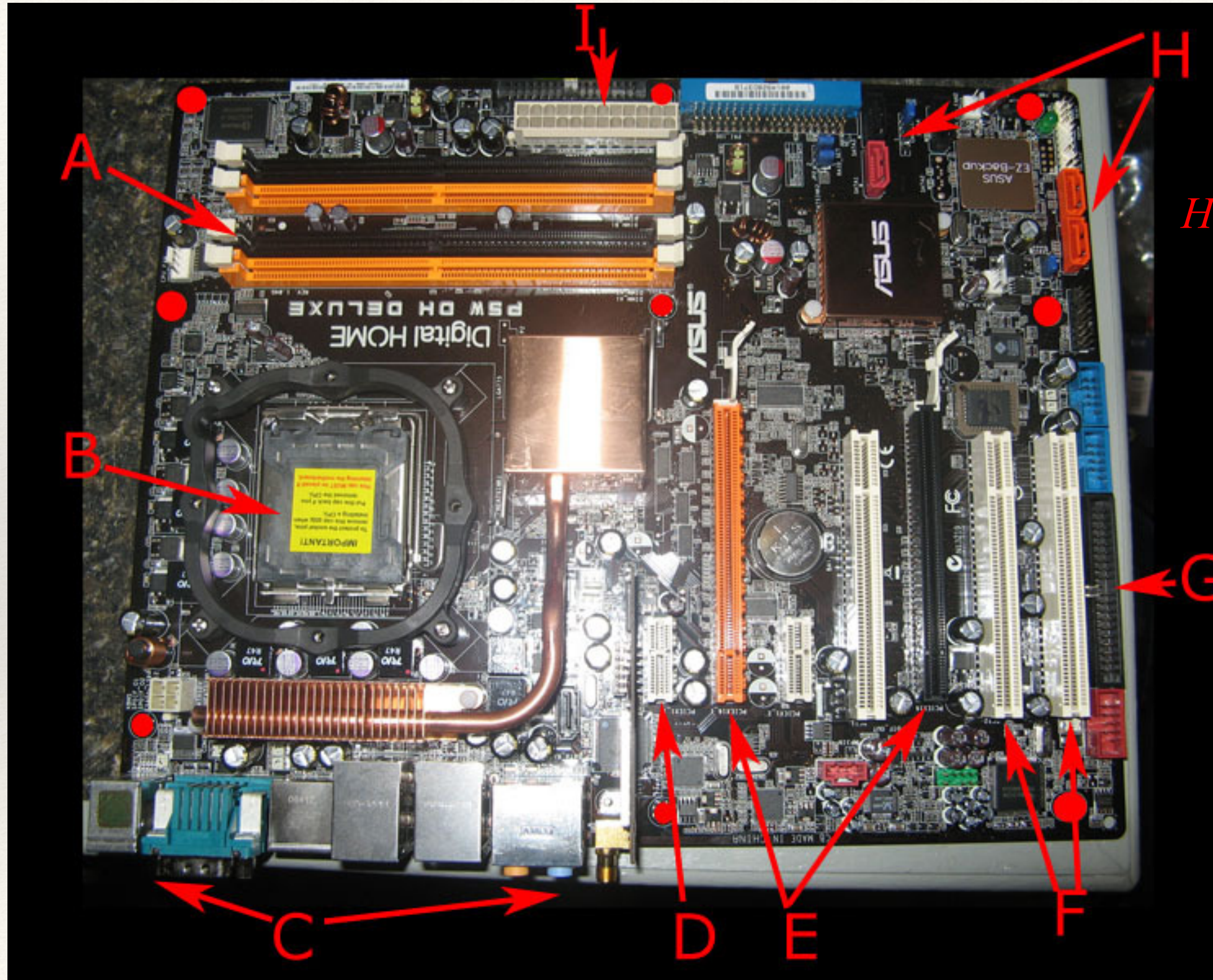
# The motherboard: backbone of the computer

*Power supply connector*

*Slot for memory:  
RAM*

*Hard drive connectors*

*Slot for CPU*



*Input/Output: Keyboard, Mouse,...*

*Extension cards: Video, sound, internet...*

# Communications on the mother board

